1 General Description

The SC32L14T/14G is an industrial-grade, ultra-low-power Flash microcontrollers based on the Arm Cortex®-M0+ core, featuring high-performance, low-power, and high-reliability applications. These microcontrollers operate at a high frequency of up to 48MHz. The Cortex®-M0+ core utilizes a 32-bit reduced instruction set architecture (RISC) and complies with the CMSIS standard. The SC32L14T/14G series offers powerful data processing capabilities, with an integrated Direct Memory Access (DMA) controller for high-speed data transfer. The hardware CRC module and the built-in 32-bit hardware multiplier further enhance the data computation speed. The embedded AES/TRNG function ensures comprehensive system security.

The SC32L14T/14G microcontrollers incorporate two clock sources: a high-precision high-frequency 48MHz oscillator (HIRC), a low-frequency 32kHz oscillator (LIRC). Additionally, they provide two external crystal oscillator interfaces: a 2-16MHz high-frequency crystal (HXT) interface and a 32.768 kHz low-frequency crystal (LXT) interface. The embedded clock sources and external crystal oscillator interfaces can supply the system clock, and the built-in system clock monitor module switches to HIRC as the clock source in case of system clock abnormalities, ensuring stable system operation.

The SC32L14T/14G series offers a wide range of peripheral resources: up to 77 GPIO pins, all pins maintain port status in sleep mode, support external interrupts, and wake-up the CPU in sleep mode; in addition, the series also has eight 16-bit timers, 1 low- power counter (LPC), 1 low-power basic timer (BTM), 8 channels of 16-bit multifunctional PWM with fault detection function; It also features 6 independent UARTs, among which UART2 features a complete LIN interface and support low-power wake-up; One 7816 SMCI; 2 multi-function communication ports (SPI0/1 & TWI0/1); built-in RTC perpetual calendar; support resistor and capacitor LCD driver mode; 32-channel high-sensitivity capacitive touch circuits; 1 analog comparator, 1 rail-to-rail OP, and 23 channels of 14-bit high-precision ADC. The microcontrollers come with an independent watchdog timer (WDT) and a highly reliable, configurable low-voltage reset circuit (LVR) to enhance system reliability. They provide three power modes to provide strong support for low-power design.

The SC32L14T/14G series delivers high performance and reliability, supporting operating voltage range of 1.8-5.5V and capable of operating stably in an ambient temperature range of -40°C to 105°C. They also exhibit excellent ESD performance and EFT immunity. In terms of process technology, the SC32L14T/14G series adopts the industry-leading eFlash process, allowing for more than 100,000 erase/write cycles and data retention of 100 years at room temperature. Regarding storage resources, the SC32L14T/14G series offers a maximum of 256 Kbytes of ROM space and 16 Kbytes of SRAM The SRAM also supports parity check functionality for enhanced system stability. Additionally, there is a 2 Kbytes user storage area (generic EEPROM), and a 4 Kbytes system storage area (LDROM). It includes a built-in system storage area to support OTA upgrades and provides multiple programming methods such as ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In-Application Programming), enabling on-board debugging and firmware updates while the chip is online or powered. This series utilizes the Cortex-M0+ core and is compatible with proven Keil & IAR debugging and development software, supporting both C and assembly language instructions.

The SC32L14T/14G series, with its exceptional low power consumption, constructs a secure environment through hardware-based AES combined with the TRNG, along with excellent anti-interference capabilities. It meets diversified requirements for secure encryption, low-power operation, high-reliability touch control, and main control integration. Its applications are extensive, covering the following fields: consumer electronics (such as interactive panels with touch/LCD for smart appliances, PC peripherals, gaming consoles, GPS devices), smart homes and IoT (such as smart controllers/thermostats, smart locks, wired/wireless sensors, remote gas/water meters), secure portable devices (such as payment terminals, medical handheld instruments, health and fitness devices, visual docking machines), and industrial control (such as industrial sensors, remote control, instruments with touch functionality, and HMI devices), among many others.

With its core advantages of security, reliability, precise interaction, and multi-scenario penetration, the SC32L14T/14G series provides a one-stop solution for high-performance, low-power MCUs, helping customers achieve intelligent, low-power, and highly reliable product design goals.

2 Features

Operating Conditions

- Operating voltage: 1.8V~5.5V
- Operating temperature: -40 ~ +105℃

EMS

- ESD
  - HBM：ANSI/ ESDA/JEDEC JS-001-2023 Class 3A
  - CDM：ANSI/ESDA/JEDEC JS-002-2022 Class C3
- EFT
  - EN61000-4-4 Level 4

Package

- 80 PIN: LQFP80 (12X12)
- 64 PIN: LQFP64 (10X10)
- 48 PIN: LQFP48 (7X7)/ QFN48 (5X5)

Core

- Cortex®-M0+ core
- With Wakeup Interrupt Controller (WIC) module
- With MPU module
- 64-bits instruction prefetch
- Built-in Multiplier Unit (MDU)

Reset

- Power-On Reset (POR)
- Software Reset
- Reset through external NRST pin (PE5) with a low-level signal
- Watchdog Timer (WDT) reset
- Low Voltage Reset (LVR)
  - Four selectable reset voltages: 4.3V, 3.7V, 2.9V, 1.7V
  - The default value is determined by the user's programmed Code Option

BUS

- 1 IOPORT
- 1 AHB
- 3 APB：APB0~APB2

Low Power Consumption

- Operation Mode: Typical operating power consumption is 150μA/MHz.
- IDLE Mode, can be woken up by any interrupt
- STOP Mode:
  - Can be woken up by INT0~15, Base Timer, TK, UART0~5, RTC, LPC and CMP
  - The typical base current in STOP Mode is as low as 1μA@ V_{DD}=5V
  - When the RTC is started in STOP Mode, the typical total current of the chip (including the LXT circuit current) is as low as 1.5μA@ V_{DD}=5V
  - When LCD display drive (no load) is enabled in STOP Mode, the typical total current of the chip is as low as 1.5μA @ V_{DD}=5V
  - Wake-up time in STOP Mode is no more than 36μs

Advanced Encryption Standard (AES)

- Support key length：128/192/256-bit
- Supports chaining modes: ECB, CBC and CTR mode
- Supports working modes: encryption/decryption
- hardware-accelerated sampling architecture, with a dedicated hardware co-processor for high-performance computation

True Random Number Generator (TRNG)

- Can generate 32-bit true random numbers
- If randomness is low, a seed error interrupt can be triggered
- Provide an interrupt when the random number generation is complete

Real-Time Clock (RTC)

- Clock source is LXT
- Can operate in low-power mode and supports wake-up from STOP Mode
- Calendar function
  - Supports BCD format time/date registers
  - Hardware automatically handles leap year corrections
  - Accuracy follows the external 32.768K LXT
- Interrupt System
  - Can set an alarm interrupt
  - Can configure fixed interrupt periods: year, month, day, hour, minute, second, or half-second (0.5 seconds)
  - Supports wake-up from STOP mode via interrupt events
- Time mode configuration
  - Supports 24-hour or 12-hour time display modes
- Secure read/write mechanism
  - Provides a half-second flag to avoid timing conflicts caused by the carry process

2.1 Flash

APROM

- Up to 256 Kbytes APROM
- Can be rewritten up to 100,000 times
- data retention of 100 years at room temperature
- Supports hardware read protection encryption
- Supports hardware write protection: Provides two regions for disabling IAP (In-Application Programming) operations. Users can configure the settings through the Code Option, with the minimum setting unit being 512 bytes (one sector)

LDROM

- 4 Kbytes of system storage area, factory-programmed with BootLoader program

SRAM

- 16 Kbytes Internal SRAM
- Supports parity check:
  - An additional 2K RAM is used for parity checking, which means SRAM data bus width is 36 bits, with 4 bits dedicated to parity check (one bit per byte)
  - The parity check bits are calculated and saved when writing to the SRAM, and automatically verified upon reading. If a bit fails, an unmaskable interrupt (Cortex®-M0+ NMI) will be generated
  - Provides an independent SRAM parity error flag, SRAMPEIF
- Supports booting from SRAM

2K Bytes User Storage Area (generic EEPROM)

- Divided into four 512 bytes sectors
- Can be rewritten up to 100,000 times
- Data retention time is over 100 years at room temperature

96 bits unique ID

- 96-bit Unique ID defined in the design option area

2.2 BootLoader

- Hardware method: System storage area of 4 Kbytes, factory-programmed with BootLoader program
- Software method: Supports interrupt vector table remapping, allowing flexible partitioning of the APROM area for user BootLoader program execution

2.3 Flash Programming and Emulation

- Programming methods supported: ICP / ISP / IAP
- 2-wire JTAG / SWD programming and emulation interface
- Simulation functionality is not supported in encrypted mode

2.4 Clock source

Built-in high-frequency 48 MHz oscillator (HIRC)

- Can be selected as the system clock source
- The default clock frequency when power on "f_{SYS}" is $f_{HIRC}/2$
- Frequency Error: Within ±1% @ -40 ~ 105℃ @ 1.8V~ 5.5V
- The system clock can be automatically calibrated by 32.768 kHz external crystal oscillator, after calibration HIRC accuracy can be infinitely close to the accuracy of external 32.768 kHz crystal oscillator

Built-in low-frequency 32 kHz oscillator (LIRC)

- Can be selected as the system clock source
- Fixed as the WDT clock source, which will be automatically enabled when WDT is enabled
- Can be selected as the Base Timer clock source and wake-up from STOP Mode
- Can be selected as the LCD clock source
- Frequency Error: Within ±4% @ 25℃ @ 1.8V~ 5.5V

External 2~16MHz crystal oscillator (HXT)

- Can be selected as the system clock source
- User can choose an external crystal oscillator oscillating frequency of <12MHz or ≥12MHz

External 32.768 kHz crystal oscillator (LXT)

- Can be selected as the system clock source
- Can be selected as the Base Timer clock source
- Can be selected as the LCD/LED clock source
- Allows for an external 32.768kHz oscillator
- Automatic calibration of HIRC can be performed using LXT

2.5 Interrupts (INT)

- Up to 27 interrupts
- Four-level interrupt priority can be set
- External interrupts (INT):
  - 16 interrupts, occupying 4 interrupt vectors in total
  - Change Interrupts on All GPIO pins
  - All interrupts can be set as rising edge, falling edge, or both-edge interrupts, each with an independent corresponding interrupt flag
  - Setting the corresponding interrupt flag in software triggers entry into the corresponding interrupt

2.6 Digital peripherals

Up to 77 GPIOs

- Independent pull-up resistor configuration is available
- IO sink current drive capability: 50mA@ V_{PIN}=0.8V
- IO source current drive capability: 12mA@ V_{PIN}=4.3V

A Two-Channel Input Low-Power Counter (LP Counter)

- Can be connected to devices such as linear or incremental encoders to obtain count, direction, and other information
- Counting in STOP mode to reduce MCU wake-up frequency and overall power consumption
- Provides two external signal input ports, INTA and INTB, which can independently detect the rising and falling edges of the input signals and count independently
  - Edge detection can trigger an interrupt
  - Count overflow can trigger an interrupt
- Direction information of the input signal can be determined by hardware
  - Direction jump can trigger an interrupt
- LPC interrupt can wake up from STOP mode

Watchdog timer (WDT)

- Built-in WDT with programmable overflow time ranging from 3.94ms to 500ms

Base Timer（BTM）

- The clock sources LXT and LIRC are selectable
- Selectable interrupt frequency intervals from 15.625ms to 32s
- Can wake up from STOP Mode

8 16-bit timers: Timer0~Timer7

- 16-bit up, down, and up/down auto-reload counters
- Supports rising edge/falling edge capture for PWM duty and period capture
- Each TIM can provide two channels of synchronized and adjustable duty cycle PWM outputs (TPWMA/TPWMB).
- TIM1/2/6 timer overflow and capture events can trigger DMA requests
- Each Tn of TIM0~7 can be mapped to another sets of IO pins

8 channels 16-bit Advanced PWM0

- The clock sources HIRC and PCLK are selectable
- Shared period and independently adjustable duty cycle
- Support dead time and complementary PWM output
- Support center-aligned mode
- Support fault detection (FTL)

6 independent UART: UART0~5

- Independent baud rate generator
- UART0~5 all support wakeup from STOP Mode
- UART0~5 ports can be mapped to 2 sets of IO pins
  - UART3 supports only half-duplex communication when mapped to programming / debugging port
- Three communication modes are optional:
  - Mode 0, 8-bit half-duplex synchronous communication mode
  - Mode 1, 10-bit full-duplex asynchronous communication
  - Mode 2, reserved
  - Mode 3, 11-bit full-duplex asynchronous communication
- UART2 has a full LIN interface, offering the following capabilities:
  - Master and slave mode switching
  - Hardware break transmission in master mode(10/13bits)
  - Hardware break detection in slave mode(10/11bits)
  - Baud rate synchronization in slave mode
- UART0 and UART1 support DMA requests
- UART2~5 do not support DMA requests

7816 Smart Card Interface (SMCI)

- The protocol complies with the ISO-7816-3 T=0 asynchronous half-duplex transmission protocol standard
- Supports Direct/Inverse Convention
- Programmable clock source frequency f_{SC}
- Flexible and adjustable basic time unit (ETU)
- Configurable Extra Guard Time
- Data frame control:
  - Supports programmable parity mode: even parity or no parity
  - Automatically generate and detect parity bits
  - Configurable stop bit length (1~2 bits)
  - Error indication signal pulse width can be set
- Supports signal port mapping

2 Advanced two in one Interface SPI0/1 & TWI0/1

- SPI0/1:
  - Supports 8-bit or 16-bit communication mode
  - Signal ports can be mapped to 3 additional set of ports Supports DMA
- TWI0/1:
  - Supports master mode or slave mode
  - Supports clock stretching in slave mode
  - Communication speed up to 1Mbps
  - Signal ports can be mapped to 3additional set of ports
  - Supports DMA

CRC

- Initial value can be set, with a default of 0xFFFF_FFFF
- Polynomial can be programmed, with a default of 0x04C1_1DB7
- Supports 8/16/32-bit data units

LCD Driver

- The clock sources LXT and LIRC are selectable
- Support display in STOP mode
- Support resistor and capacitor bias voltage generating circuit
- Resistor LCD driver supports fast charge mode, LCD voltage output port voltage divider resistor options: 11KΩ, 100KΩ, 300KΩ, 800KΩ
- Capacitive LCD driver is in capacitive bias mode. In this mode, the total power consumption of the LCD circuit can be as low as: 2~3μA @STOP mode
- LCD:
  - Supports 8 X 51, 6 X 53, 5 X 54, or 4 X 55 segment LCD driving
  - Two bias voltages options: 1/3 and 1/4
  - Two waveform modes: Type A and Type B
  - Three frame frequencies available:
    - 32/64/128 Hz in Type A mode
    - 64/128/256 Hz in Type B mode

DMA

- 2 independent configurable channels
- Each DMA channel can send DMA requests to other channels
- Data width supports byte, half-word, and word
- 20 DMA request sources with two priority levels
- Supports source/destination address auto-increment or fixed
- Supports single and burst transfer modes
- Transfer modes: memory to memory, memory to peripheral, peripheral to memory, peripheral to peripheral

2.7 Analog peripherals

Low Voltage Detector (LPD):

- 8-level low-voltage detection:
  - 1.85V / 2.05V / 2.25V / 2.45V / 2.65V / 2.85V / 3.05V / 3.25V
- Can generate interrupts
- The power supply of LPD is turned off in STOP mode

32-channel high-sensitivity Touch Key circuit

- Only supported by SC32L14T series
- Channels can be scanned in parallel
- 103 Capacitor must be connected between the CMOD pin and ground
- Has strong anti-interference ability and can pass 10V dynamic CS test
- Supports self-capacitance mode and mutual-capacitance mode
- Supports low-power mode
- Supports fast wake-up STOP mode
- Suitable for touch applications with high sensitivity requirements, such as proximity sensing and touch keys
- Comprehensive development support: Highly flexible touch software library, intelligent debugging software

Analog-to-Digital Converter ADC

- Precision: 14 bits
- Supports up to 23 channels
  - External 20 ADC sampling channels can be multiplexed with I/O ports for other functions
  - One internal ADC can directly measure V_{DD} voltage
  - One internal ADC can directly measure OP output
  - One internal temperature sampling channel
- Four options for ADC reference voltage: V_{DD}, and internal 2.048V, 1.024V, or 2.4V
- Configurable ADC conversion completion interrupt
- Supports single-channel continuous conversion mode
- Supports DMA transmission: DMA request will be generated after ADC conversion complete
- The conversion results feature an overflow flag: OVERRUN, and the OVERRUN flag bit is in the same register as the ADC conversion results so users can read the information all at once

Operational Amplifier (OP)

- A rail-to-rail input stage
- Can be configurable as a Programmable Gain Amplifier (PGA)
  - Non-inverting gain: 8/16/32/64
  - Inverting gain: 7/15/31/63
- Two external pins for the non-inverting input: OP_P0 or OP_P1
- One external pin for the inverting input: OP_N
- One external pin for the output: OP_O
- The output can be directly connected to the ADC input
- The output can be directly connected to the positive input of a Comparator (CMP)

Analog Comparator CMP

- Five positive input signals selectable:
  - Four analog signal positive input terminals: CMP0~CMP3
  - OP output signal
- Negative input voltage can be selected from CMPR input or one of the 15 comparison voltages derived from the internal V_{DD} voltage division
- CMP interrupts can wake up the STOP mode

Temperature Sensor

- The voltage value of temperature sensor can be measured by ADC
- Use internal 2.4V as reference voltage
- The conversion value of ADC will increase by a fixed value for every increase of 1℃

Product Peripheral Resource Table

Model Peripherals	SC32L14T_ SC32L14G_					
	_M8	_R8	_C8	_M7	_R7	_C7
GPIOs	77	61	45	77	61	45
APROM (Kbyte)	256			128		
SRAM (Kbyte)	16					
TK	SC32L14T_(with TK) & SC32L14G_(without TK)					
SPI	2	2	2	2	2	2
TWI	2	2	2	2	2	2
UART	6	5	2	6	5	2
7816 SMCI	1	1	0	1	1	0
TIM	8	8	7	8	8	7
LPC	1	1	1	1	1	1
RTC	1	1	1	1	1	1
PWM0	8	8	8	8	8	8
AES	1	1	1	1	1	1
TRNG	1	1	1	1	1	1
OP	1	1	\	1	1	\
CMP	1	1	\	1	1	\
ADC Channels	23	18	16	23	18	16
LCD COM X SEG	8X51 6X53 5X54 4X55	8X36 6X38 5X39 4X40	8X24 6X26 5X27 4X28	8X51 6X53 5X54 4X55	8X36 6X38 5X39 4X40	8X24 6X26 5X27 4X28
CRC	YES					
DMA	YES					
LPD	YES					
Temperature Sensor	YES					
Max. CPU frequency	48MHz					

Ordering Information

PRODUCT ID	PACKAGE	PACK
SC32L14TM8PJR	LQFP80	TRAY
SC32L14TM7PJR	LQFP80	TRAY
SC32L14GM8PJR	LQFP80	TRAY
SC32L14GM7PJR	LQFP80	TRAY
SC32L14TR8PJR	LQFP64	TRAY
SC32L14TR7PJR	LQFP64	TRAY
SC32L14GR8PJR	LQFP64	TRAY
SC32L14GR7PJR	LQFP64	TRAY
SC32L14TC8PJR	LQFP48	TRAY
SC32L14TC7PJR	LQFP48	TRAY
SC32L14GC8PJR	LQFP48	TRAY
SC32L14GC7PJR	LQFP48	TRAY
SC32L14TC8QJR	QFN48	TRAY
SC32L14TC7QJR	QFN48	TRAY
SC32L14GC8QJR	QFN48	TRAY
SC32L14GC7QJR	QFN48	TRAY

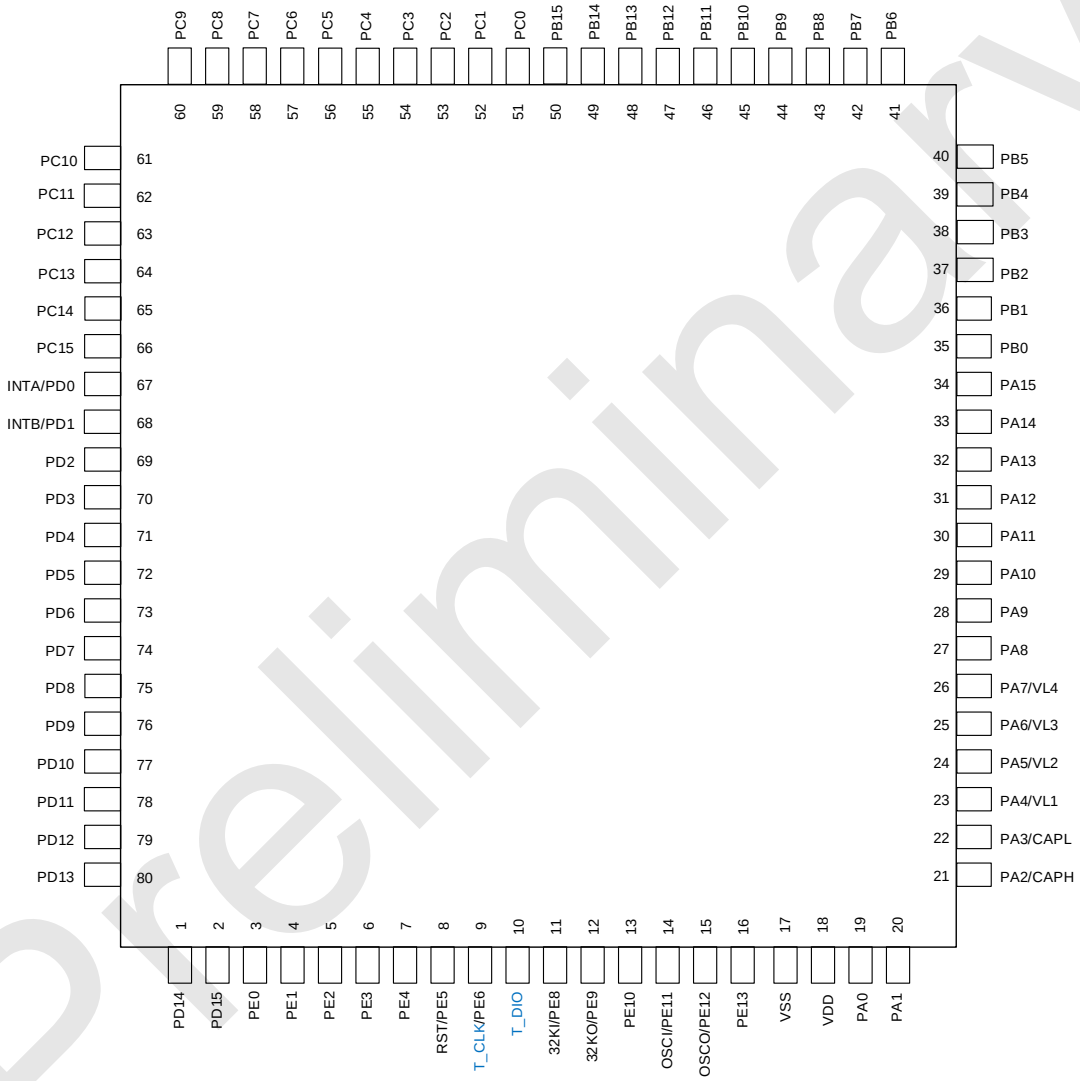
Note: Regarding the mass production status of specific models, please consult sales representatives from SinOne or authorized distributors for information on sample availability and lead times before starting development.

Content

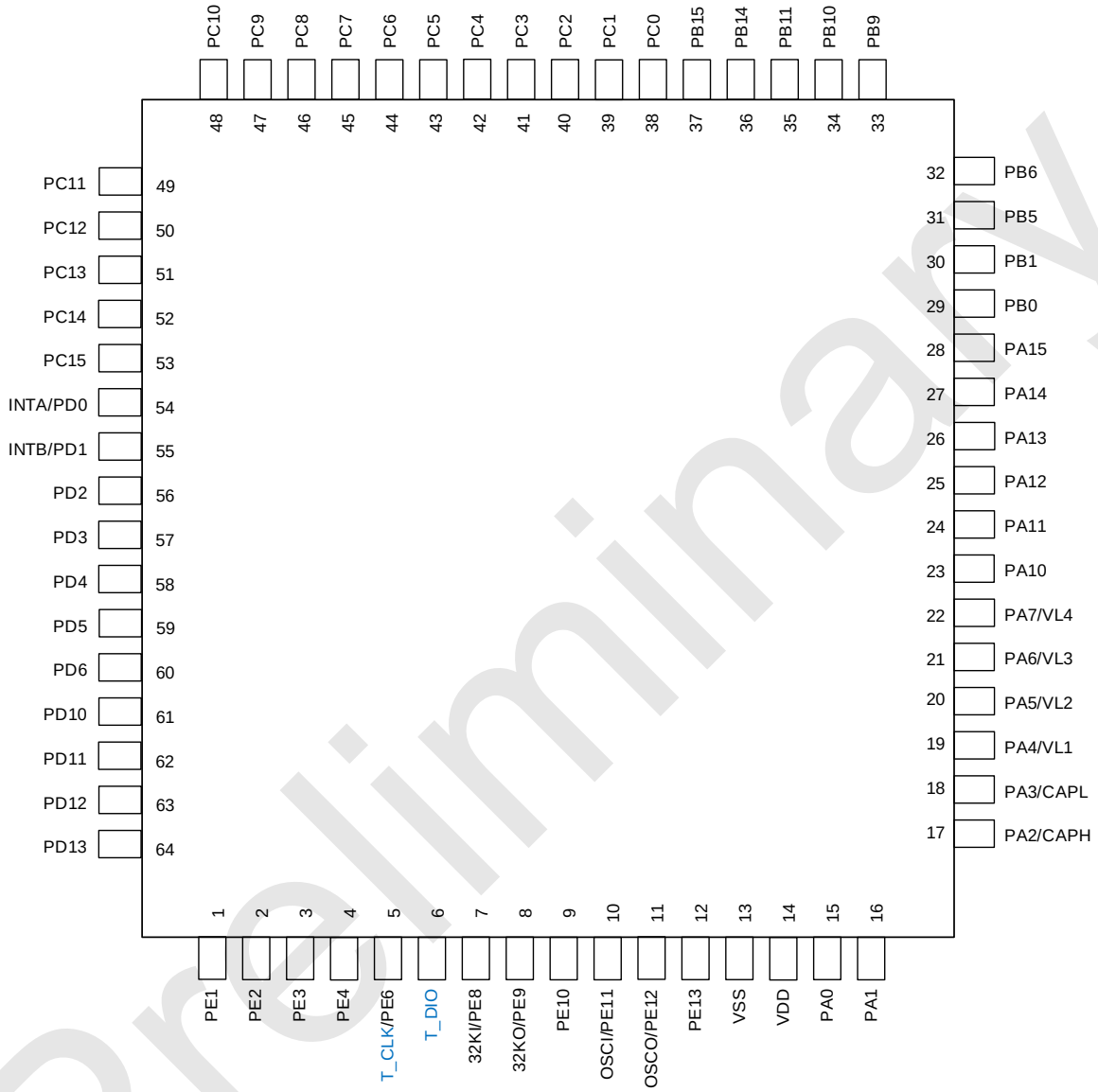
3 Pin Description

3.1 Pin Configuration

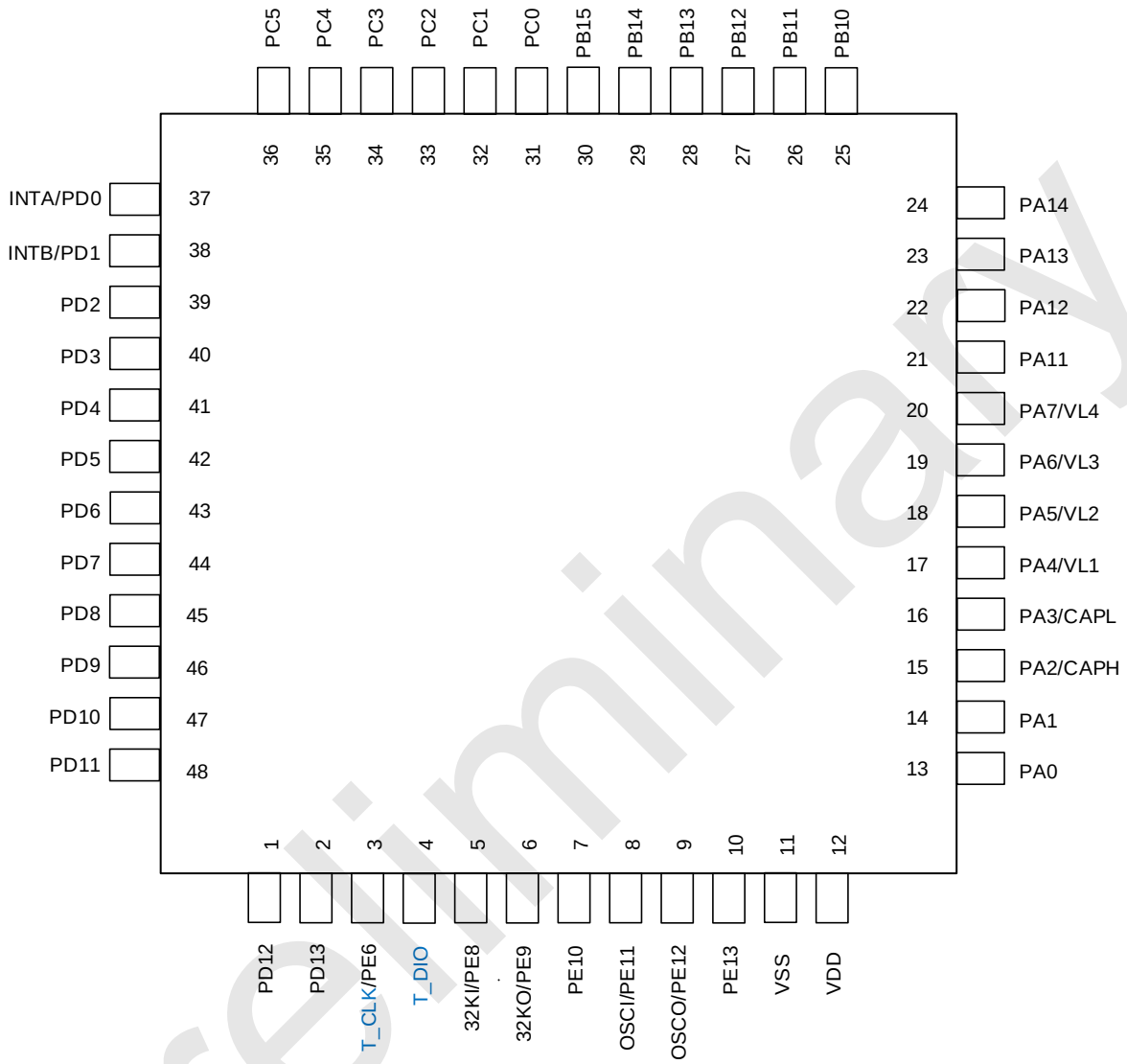
Note: TK function is only supported on the SCL14T series.



80PIN Pin Diagram
Suitable for LQFP80 package



64PIN Pin Diagram
Suitable for LQFP64 package



48PIN Pin Diagram
Suitable for LQFP48, QFN48 package

3.2 Pin Resource List

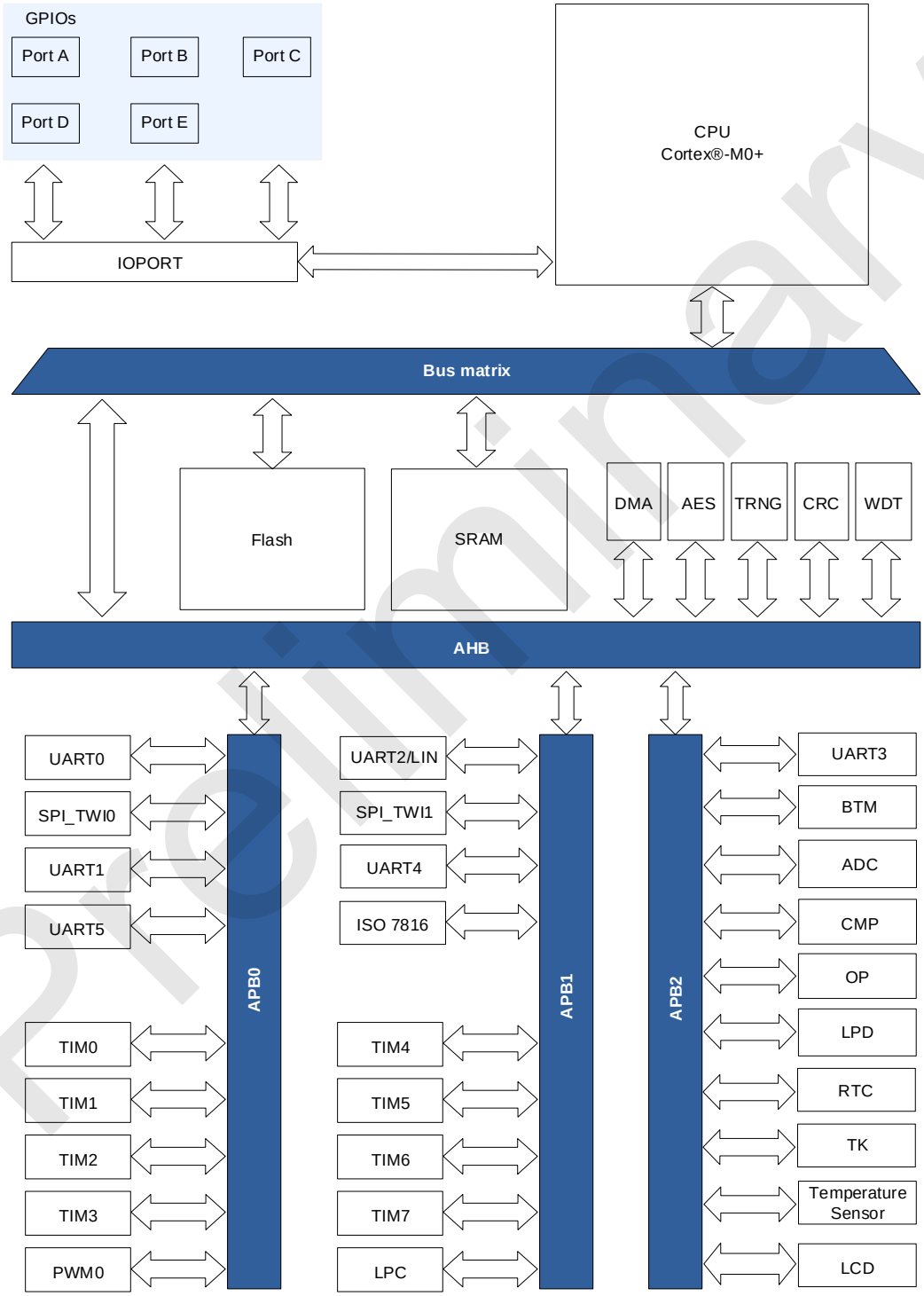
LQFP48/ QFN48	LQFP64	LQFP80	GPIO	特殊	UART	TWI	SPI	LCD	TK	ADC	PWM-8	PWM	TxEX/Tx	CMP	OP	INT
-	-	1	PD14		(TxD2)		(MISO0A)	SEG30	TK0	AIN19		T7PWM1	T7EX			INT14
-	-	2	PD15		(RxD2)	(SDA0A)	(MOSI0A)	SEG29	TK1	AIN18						INT15
-	-	3	PE0			(SCL0A)	(SCK0A)	SEG28	TK2					CMPR		INT0
-	1	4	PE1						TK3					CMP3	OP_N	INT1
-	2	5	PE2			(SCL1A)	(SCK1A)		TK4					CMP2	OP_P0	INT2
-	3	6	PE3		(RxD1)	(SDA1A)	(MOSI1A)		TK5					CMP1	OP_P1	INT3
-	4	7	PE4		(TxD1)		(MISO1A)		TK6			T5PWM0	T5CAP/T5	CMP0	OP_0	INT4
-	-	8	PE5	RST								(T7PWM0)	(T7CAP/T7)			INT5
3	5	9	PE6	T_CLK	RxD3							(T0PWM0)	(T0CAP/T0)			INT6
4	6	10	-	T_DIO	TxD3											-
5	7	11	PE8	32KI							PWM0_3					INT8
6	8	12	PE9	32KO							PWM0_2					INT9
7	9	13	PE10								PWM0_1					INT10
8	10	14	PE11	OSCI							PWM0_0					INT11
9	11	15	PE12	OSCO												INT12
10	12	16	PE13				(MISO0B)		CMOD							INT13
11	13	17	VSS	VSS												
12	14	18	VDD	VDD												
13	15	19	PA0			（SDA0B）	(MOSI0B)	SEG27				(T2PWM0)	(T2CAP/T2)			INT0
14	16	20	PA1			（SCL0B）	(SCK0B)	SEG26				(T1PWM0)	(T1CAP/T1)			INT1
15	17	21	PA2	CAPH								(T3PWM0)	(T3CAP/T3)			INT2
16	18	22	PA3	CAPL								(T4PWM0)	(T4CAP/T4)			INT3

LQFP48/ QFN48	LQFP64	LQFP80	GPIO	特殊	UART	TWI	SPI	LCD	TK	ADC	PWM-8	PWM	TxEX/Tx	CMP	OP	INT
17	19	23	PA4	VL1							PWM0_4					INT4
18	20	24	PA5	VL2							PWM0_5					INT5
19	21	25	PA6	VL3							PWM0_6					INT6
20	22	26	PA7	VL4							PWM0_7	(T6PWM0)	(T6CAP/T6)			INT7
-	-	27	PA8		TxD1			SEG25								INT8
-	-	28	PA9		RxD1			SEG24								INT9
-	23	29	PA10			(SCL1B)	(SCK1B)	SEG23								INT10
21	24	30	PA11			(SDA1B)	(MOSI1B)	SEG22	TK7			T1PWM0	T1CAP/T1			INT11
22	25	31	PA12				(MISO1B)	SEG21	TK8							INT12
23	26	32	PA13					SEG20	TK9			T3PWM0	T3CAP/T3			INT13
24	27	33	PA14		(RxD0)			SEG19	TK10							INT14
-	28	34	PA15		(TxD0)			SEG18	TK11							INT15
-	29	35	PB0					SEG17	TK12							INT0
-	30	36	PB1					SEG16	TK13							INT1
-	-	37	PB2					SEG15								INT2
-	-	38	PB3		RxD4			SEG14								INT3
-	-	39	PB4		TxD4			SEG13								INT4
-	31	40	PB5					SEG12			FLT					INT5
-	32	41	PB6					SEG11				T6PWM1	T6EX			INT6
-	-	42	PB7		(RxD5/SCCLK0)			SEG10				T6PWM0	T6CAP/T6			INT7
-	-	43	PB8		(TxD5/SCIO0)			SEG9				T2PWM1	T2EX			INT8
-	33	44	PB9		RxD5/SCCLK0			SEG8				T2PWM0	T2CAP/T2			INT9

LQFP48/ QFN48	LQFP64	LQFP80	GPIO	特殊	UART	TWI	SPI	LCD	TK	ADC	PWM-8	PWM	TxEX/Tx	CMP	OP	INT
25	34	45	PB10		TxD5/SCIO0			SEG7				T0PWM1	T0EX			INT10
26	35	46	PB11				(MISO1C)	SEG6				T0PWM0	T0CAP/T0			INT11
27	-	47	PB12			(SDA1C)	(MOSI1C)	SEG5								INT12
28	-	48	PB13			(SCL1C)	(SCK1C)	SEG4								INT13
29	36	49	PB14					COM7/SEG3								INT14
30	37	50	PB15					COM6/SEG2								INT15
31	38	51	PC0					COM5/SEG1								INT0
32	39	52	PC1					COM4/SEG0								INT1
33	40	53	PC2					COM3								INT2
34	41	54	PC3					COM2								INT3
35	42	55	PC4					COM1								INT4
36	43	56	PC5					COM0								INT5
-	44	57	PC6		(TxD3)		MISO0	SEG54				T1PWM1	T1EX			INT6
-	45	58	PC7		(RxD3)	SDA0	MOSI0	SEG53								INT7
-	46	59	PC8			SCL0	SCK0	SEG52								INT8
-	47	60	PC9		TxD0			SEG51								INT9
-	48	61	PC10		RxD0			SEG50								INT10
-	49	62	PC11					SEG49				T5PWM1	T5EX			INT11
-	50	63	PC12					SEG48	TK14	AIN17		(T5PWM0)	(T5CAP/T5)			INT12
-	51	64	PC13		TxD2		MISO1	SEG47	TK15	AIN16						INT13
-	52	65	PC14		RxD2	SDA1	MOSI1	SEG46	TK16	AIN15						INT14
-	53	66	PC15			SCL1	SCK1	SEG45	TK17	AIN14						INT15
37	54	67	PD0	INTA				SEG44	TK18	AIN13		T7PWM0	T7CAP/T7			INT0
38	55	68	PD1	INTB				SEG43	TK19	AIN12		T4PWM0	T4CAP/T4			INT1
39	56	69	PD2					SEG42	TK20	AIN11						INT2

LQFP48/ QFN48	LQFP64	LQFP80	GPIO	特殊	UART	TWI	SPI	LCD	TK	ADC	PWM-8	PWM	TxEX/Tx	CMP	OP	INT
40	57	70	PD3					SEG41	TK21	AIN10						INT3
41	58	71	PD4					SEG40	TK22	AIN9						INT4
42	59	72	PD5					SEG39	TK23	AIN8						INT5
43	60	73	PD6					SEG38	TK24	AIN7						INT6
44	-	74	PD7		(TxD4)		(MISO0C)	SEG37	TK25	AIN6						INT7
45	-	75	PD8		(RxD4)	（SDA0C）	(MOSI0C)	SEG36	TK26	AIN5						INT8
46	-	76	PD9			（SCL0C）	(SCK0C)	SEG35	TK27	AIN4						INT9
47	61	77	PD10					SEG34	TK28	AIN3		T4PWM1	T4EX			INT10
48	62	78	PD11					SEG33	TK29	AIN2		T3PWM1	T3EX			INT11
1	63	79	PD12					SEG32	TK30	AIN1						INT12
2	64	80	PD13					SEG31	TK31	AIN0						INT13

4 Resource Diagram

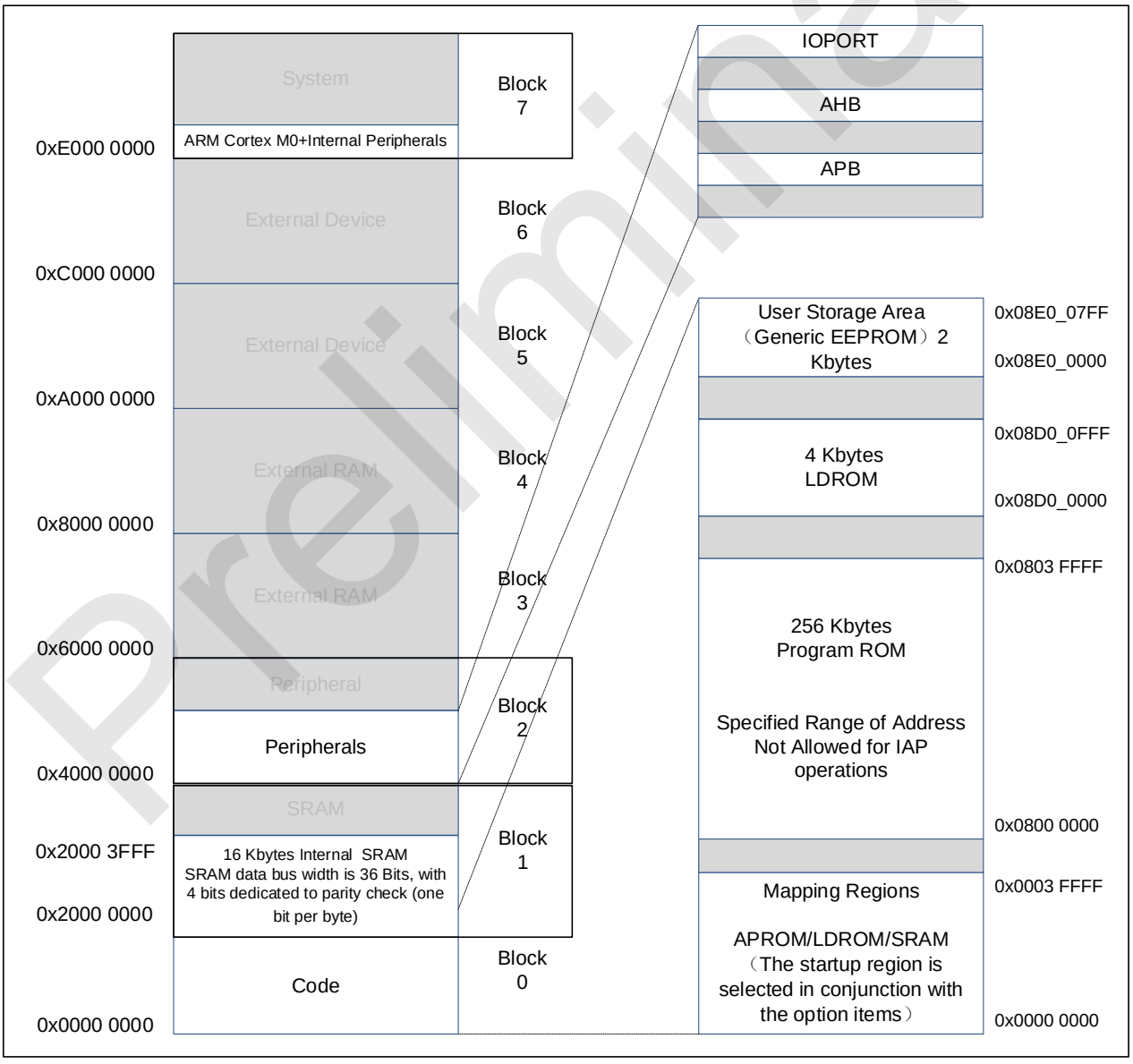


5 Flash

5.1 Overview

The program memory, data memory, and registers are arranged within a single linear (i.e., contiguous) 4 GB address space. Each byte is encoded in the storage in little-endian format, meaning that the least significant byte of a word is the lowest numbered byte, while the most significant byte is the highest numbered byte. The addressable storage space is divided into 8 main blocks, each block being 512 MB in size.

5.2 Storage Block Diagram



SC32L14T/14G Series Memory Mapping Diagram

5.3 Feature

- The Flash width is 32 bits, and it can be rewritten up to 100,000 times
- Data retention time is over 100 years at room temperature
- The structure of the Flash includes:
  - Maximum 256 Kbytes APROM
  - 4 Kbytes LDROM
  - 2 Kbytes user storage area (generic EEPROM)
  - 16 Kbytes Internal SRAM, support parity check
  - 96 bits Unique ID

5.4 APROM

- APROM of SC32L14xx8 series has 256K bytes
- APROM of SC32L14xx7 series has 128K bytes
- Sector Size: 512 bytes
- Supports: Read/Write/Sector Erase/Chip Erase/Blank Check
- The CPU (Cortex®-M0+) accesses Flash through the AHB bus
- The program defaults to booting from APROM, and users can select programs to boot from other areas such as SRAM/LDROM using the customer option OP_BL[1:0]
- Read Protection: After enabling read protection, only a program that runs from APROM can read information from APROM. Other areas or third-party tools cannot access information from APROM
- Write Protection: Provides two hardware write protection regions where IAP operations are prohibited. Users can set the range of the two write protection regions in units of sectors based on actual needs

The 256 Kbytes of APROM is divided into 512 sectors, with each sector being 512 bytes. During programming, the sector to which the target address belongs will be forcibly erased by the programmer before writing data. During user write operations, the sector must be erased first before writing data.

SC32L14T 256 Kbytes Flash ROM Sector Partition Illustration

The 128 Kbytes of APROM is divided into 256 sectors, with each sector being 512 bytes. During programming, the sector to which the target address belongs will be forcibly erased by the programmer

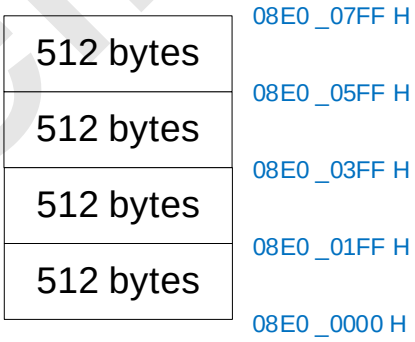
before writing data. During user write operations, the sector must be erased first before writing data.

SC32L14xx7 series 128 Kbytes APROM Sector Partition Illustration

5.5 2 Kbytes User Storage Area (Genetic EEPROM)

The 2K bytes of independent EEPROM area is addressed from 0x08E0_0000 H to 0x08E0_07FF H, as set by the IAPADE register. This independent EEPROM can be written to repeatedly up to 100,000 times, and it is designed to retain data for over 100 years at room temperature. The independent EEPROM supports various operations including blank check, programming, verification, erasure, and reading functions.

EEPROM has 4 sectors, with each sector being 512 bytes.



SC32L14T EEPROM Sector Partition Illustration

Note: The EEPROM has a write cycle endurance of 100,000 times. Users should avoid exceeding the rated write cycles of the EEPROM to prevent any anomalies!

5.6 4 Kbytes LDROM

- 4 Kbytes of system storage area, factory-programmed with BootLoader program, Users cannot modify or access this area

- Embedded Bootloader Program: The fixed ISP program is publicly available, allowing reprogramming of Flash via UART. The program waits for upgrade commands, and if no update command is received within 500 milliseconds, it jumps to APROM for execution (0X0800 0000)

5.6.1 BootLoader

Supports two Bootloader modes:

- Software Approach: Directly partition BootLoader and APP areas in software. Easy sharing interrupts of BootLoader and APP by modifying VTOR. Flexible adjustment of the size of each area
- Hardware Approach: 4 Kbytes fixed "LDROM" as a dedicated BootLoader area that users cannot read or write
  - LDROM serves as a fixed BootLoader space with factory-programmed program, and users cannot read or write
  - Embedded Bootloader Program: The embedded bootloader program resides in LDROM and is programmed during the production stage. The fixed ISP program is publicly available, allowing reprogramming of Flash via UART

5.7 SRAM

- Internal SRAM：16 Kbytes， address 0x2000 0000 ~ 0x2000 3FFF
- Supports parity check
  - An additional 2Kbytes RAM is used for parity checking, which means SRAM data bus width is 36 bits, with 4 bits dedicated to parity check (one bit per byte)
  - The parity check bits are calculated and saved when writing to the SRAM, and automatically verified upon reading. If a bit fails, an unmaskable interrupt (Cortex®-M0+ NMI) will be generated
  - Provides an independent SRAM parity error flag, SRAMPEIF

Note: When SRAM parity check is enabled, it is recommended to perform a software initialization of the entire SRAM at the beginning of the code to prevent parity check errors when reading from uninitialized locations.

- Users can choose to start the program from SRAM by configuring the customer option OP_BL[1:0]
- It supports byte, half-word (16-bit), or word (32-bit) access at the maximum system clock frequency, with no waiting states. Therefore, it can be accessed by both the CPU and DMA

5.8 Boot Area Selection (Bootstrap)

After a reset, users can independently configure the desired bootstrap mode.

After exiting the standby mode, the startup mode configuration can be resampled. Once this startup delay has ended, the CPU will fetch the stack top value from address 0x00000000 and then begin executing code from the bootstrap memory starting at 0x00000004.

There are three options for bootstrap area selection: Main Flash Memory Area, System Flash Memory Area and SRAM, described in detail as follows:

5.8.1 Bootstrap from APROM

APROM is aliased in the bootstrap memory space (0x00000000) but can also be accessed from its original memory space (0x08000000). In other words, the program can start accessing from either address 0x00000000 or 0x08000000.

5.8.2 Bootstrap from LDROM

- 4 Kbytes LDROM serves as a fixed BootLoader space with factory-programmed program, Users cannot modify or access this area
- Embedded Bootloader Program: The embedded bootloader program resides in LDROM and is programmed during the production stage. The fixed ISP program is publicly available, allowing reprogramming of Flash via UART

5.8.3 Bootstrap from SRAM

SRAM has an alias in the bootstrap memory space (0x0000 0000) but can also be accessed from its original memory space (0x2000 0000).

5.8.4 Bootstrap mode configure

The bootstrap modes can be controlled by the register bits BTLD[1:0] in conjunction with the software reset (RST) control bit, both protected by the IAP_KEY:：

① Set BTLD[1:0]=0x00: the chip boots from APROM after a software reset.
② Set BTLD[1:0]=0x01: the chip boots from LDROM after a software reset.
③ Set BTLD[1:0]=0x10: the chip boots from SRAM after a software reset.

The initial boot region selection during power-up can be configured by customer option bits OP_BL[1:0]:

① Set OP_BL[1:0]=0x00 in customer option: the chip boots from APROM after a software reset.
② Set OP_BL[1:0]=0x01 in customer option: the chip boots from LDROM after a software reset.
③ Set OP_BL[1:0]=0x10 in customer option: the chip boots from SRAM after a software reset.

5.9 96 bits Unique ID

The SC32L14T provides an independent Unique ID area. A 96-bit unique code can be pre-programmed before leaving the factory to ensure the uniqueness of the chip. The only way for the user to obtain the serial number is to read through the IAP instruction.

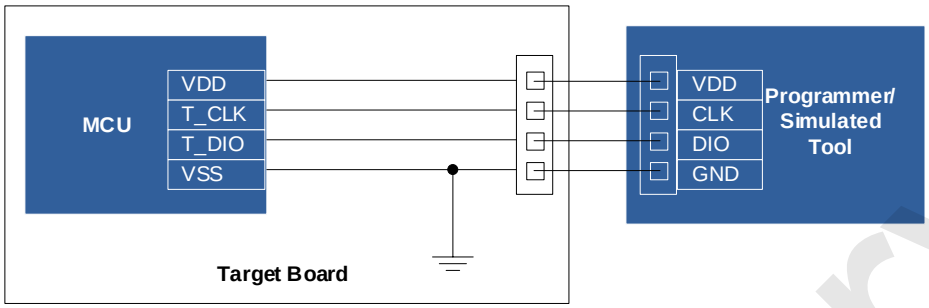
5.10 User ID Area

User ID area, where user-customized ID is pre-programmed when leaving the factory. Users can read the User ID area, but cannot write the User ID area.

5.11 Programming

The SC32L14T/14G's Flash can be programmed through T_DIO, T_CLK, VDD, VSS, the specific connection

relationship is as follows:



ICP mode Flash Writer programming connection diagram

T_DIO、T_CLK is a 2-wire JTAG programming and emulation signal line. Users can configure the mode of these two ports through the Customer Option when programming.

Note: Ports of UART3 support two mapping schemes:

- Mapping 1: RXD3 / TXD3
- Mapping 2: RXD3A / TXD3A

When Mapping 1 (RXD3/TXD3) is selected, these pins are multiplexed with the system's programming/debug interface (T_CLK / T_DIO). Under this mapping, if full-duplex communication is enabled, T_CLK / T_DIO might conflict with the receive timing of UART3's RXD3, leading to communication abnormalities. Therefore, when selecting Mapping 1, UART3 must be configured for half-duplex communication mode to avoid this hardware conflict and ensure communication stability.

If full-duplex UART communication is required, please map the pins to Mapping 2 (RXD3A/TXD3A).

5.11.1 JTAG Specific Mode

T_DIO,T_CLK are specific port for programming and emulation, and other functions multiplexed with it are not available. This mode is generally used in the online debugging stage, which is convenient for users to simulate and debug. After the JTAG special mode takes effect, the chip can directly enter the programming or emulation mode without powering on and off again.

5.11.2 Normal Mode (JTAG specific port is invalid)

The JTAG function is not available, and other functions multiplexed with it can be used normally. This mode can prevent the programming port from occupying the MCU pins, which is convenient for users to maximize the use of MCU resources.

Note: When the invalid configuration setting of the JTAG dedicated port is successful, the chip must be completely powered off and then on again to enter the programming or emulation mode, which will affect the programming and emulation in the live mode. SinOne recommends that users select the invalid configuration

of the JTAG dedicated port during mass production and programming, and select the JTAG mode during the development and debugging phase.

Related Customer Option is as followed:

Register	R/W	Description	Reset Value
COPT1_CFG@0xC2	R/W	Customer Option Mapping Register 1	0x0000_0000

7	6	5	4	3	2	1	0
ENWDT	DISJTG	DISRST	-	-	-	OP_BL[1:0]	

Bit number	Bit Mnemonic	Description
6	DISJTG	JTAG Ports Switch Control Bit 0: JTAG mode enabled, the corresponding pins can only be used as T_CLK and T_DIO 1: Normal mode, JTAG function disabled

5.12 Security Encryption

- The SC32L14T/14G series mainly involves encrypting the APROM for read protection. Users can configure the read protection encryption feature during programming through the customer option in the dedicated programming host; enable flash read protection can enter encryption mode: The chip defaults to a non-encrypted state while leaving the factory
- The read protection encryption feature has no mapped registers. Users can only modify it after config the customer option in the dedicated programming host and programming
- Encryption Disabled: Operations such as reading, programming, and erasing can be performed on APROM. These operations can be also performed on Bytes and backup registers
- Encryption Enabled:
  - Enable from APROM: Code executed in user mode (booting from user APROM) can perform all operations on APROM
  - Debug, enable from SRAM and LDROM: In debug mode or when code is booted from SRAM or LDROM, APROM is completely inaccessible
- Disabling encryption requires a full erase operation on APROM

5.12.1 Security Encryption Access Rights

Boot Area/Tools	Encryption Disabled Status					Read Protection Encryption Status				
	Read	Write	Block Erase	Full Erase	Operate Write-Protection Region	Read	Write	Block Erase	Full Erase	Operate Write-Protection Region
Bootstrap from APROM	√	√	√	\	Forbid	√	√	√	\	Forbid

Boot Area/Tools	Encryption Disabled Status					Read Protection Encryption Status				
	Read	Write	Block Erase	Full Erase	Operate Write-Protection Region	Read	Write	Block Erase	Full Erase	Operate Write-Protection Region
Debug/Bootstrap from SRAM	√	√	√	√	Forbid	Forbid	Forbid	Forbid	Forbid	Forbid
Bootstrap from LDROM	√	√	√	√	√	Forbid	Forbid	Forbid	√	Forbid

5.13 In Application Programming (IAP)

The IAP (In Application Programming) area in the APROM of SC32L14T/14G allows users to perform remote program updates through IAP operations. Users can also retrieve information from the Unique ID or User ID areas by IAP read operations. Before performing IAP write operations, users must carry out sector erasure for the target address sector.

The chip allows global IAP operations in the APROM by default while leaving the factory. Internally, the chip provides two sets of flash write protection regions. These regions are set based on sector units, and the protected areas are restricted from IAP operations. The rules for setting these regions are as follows:

IAPPORx Register Value (x=A or B)	IAPPOR Protection Area
IAPPORx_ST = IAPPORx_ED	Sector IAPPORx
IAPPORx_ST > IAPPORx_ED	No protection
IAPPORx_ST < IAPPORx_ED	Sectors from IAPPORx_ST to IAPPORx_ED

User can configure the two APROM write-protected areas via "Flash sectors protection" in the Customer Option item while programming.

Note: IAP does not support byte/half-word programming, which means IAP write operations must be word-aligned (4-byte alignment). If written by byte or half-word, the data will automatically be repeated and padded to word alignment. For example, writing 0x12 will be automatically padded and written as 0x12121212, and writing 0x1234 will be automatically padded and written as 0x12341234.

5.13.1 IAP Operation Register Table

IAP operations on APROM outside the write-protected area can be achieved through the following registers:

5.13.1.1 Data protection register IAP_KEY

Register	R/W	Description	Reset Value
IAP_KEY	R/W	Data Protection Register	0x0000_0000

31	30	29	28	27	26	25	24
IAPKEY[31:24]							

23	22	21	20	19	18	17	16
IAPKEY[23:16]							
15	14	13	12	11	10	9	8
IAPKEY[15:8]							
7	6	5	4	3	2	1	0
IAPKEY[7:0]							

Bit number	Bit Mnemonic	Description
31~0	IAPKEY[31:0]	Data Protection Key To prevent accidental operations on Flash due to electrical interference, IAP_CON Register requires unlocking through IAPKEY before performing a write operation. The unlocking sequence is as follows: 1. Write KEY1 = 0x1234_5678 2. Write KEY2 = 0xA05F_05FA The IAP_CON Register will be locked until the next system reset if the sequence of operations is incorrect.

5.13.1.2 IAP Sector Number Setting Register IAP_SNB

Register	R/W	Description	Reset Value
IAP_SNB	R/W	IAP Sector Number Setting Register	0x0000_0000

31	30	29	28	27	26	25	24
IAPADE[7:0]							
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	IAPSNB[9]	IAPSNB[8]
7	6	5	4	3	2	1	0
IAPSNB[7:0]							

Bit number	Bit Mnemonic	Description
31~24	IAPADE[7:0]	IAP Operation Area Extended Address By writing different values to IAPADE, the IAP operations can be directed to different operation areas: 0x00: Invalid 0x4C: APROM 0x69: EEPROM 0xF1: customer option

9~0	IAPSNB[9:0]	IAP Operation Sector Number Setting for Sector/Page Erase: The actual starting address of the operated sector = Flash Base Address + [IAPSNB[9:0] * 0x200]
23~10	-	Reserved

5.13.1.3 IAP Control Register IAP_CON (Write Protect)

*This register is write-protected and must be modified using the data protection register IAP_KEY

Register	R/W	Description	Reset Value
IAP_CON	R/W	IAP Control Register	0x0000_0000

31	30	29	28	27	26	25	24
LOCK	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	BTLD[1:0]		RST
7	6	5	4	3	2	1	0
ERASE	-	SERASE	PRG	-	-	CMD[1:0]	

Bit number	Bit Mnemonic	Description
31	LOCK	The IAP_CON will be locked after setting this bit to 1. When the unlock sequence is detected, this bit will be cleared by hardware, if the unlock operation fails, this bit will remain 1 until the next system reset.
10~9	BTLD[1:0]	Boot Area Selections Bit After Software Reset: 00: Boot from APROM after software reset 01: Boot from LDROM after software reset 10: Boot from embedded SRAM after software reset 11: Reserved
8	RST	Software Reset Control Bit: 0: Program running normally 1: System will reset immediately after setting this bit to 1
7	ERASE	All Erase Control Bit 0: No erase operation 1: Setting 1 to this bit and configure CMD[1:0]=10 will initiate a full erase operation on APROM.
5	SERASE	Sector Erase Control Bit: 0: No erase operation

Bit number	Bit Mnemonic	Description
		1: Setting 1 to this bit and configure CMD[1:0]=10 will initiate a sector erase operation on APROM, and the selected sector will be erased.
4	PRG	Program Control Bit: 0: Disable Flash Programming 1: Enable Flash Programming
1~0	CMD[1:0]	IAP Command Enable Control Bit: 10: Execute the erase operation command Others: Reserved **Note:** 1. The corresponding operation will execute only when CMD[1:0] set to 10 after setting any erase control bit to 1. 2. Only one IAP operation can be executed at a time, so the ERASE/SERASE bit can only be set to 1 at a time
30~11 6 3~2	-	Reserved

5.13.2 IAP Register Mapping

Register	Offset Address	R/W	Description	Reset Value
IAP Base Address:0x4000_03C0				
IAP_KEY	0x00	R/W	Data protect Register	0x0000_0000
IAP_SNB	0x04	R/W	IAP Sector Number Setting Register	0x0000_0000
IAP_CON	0x0C	R/W	IAP Control Register	0x0000_0000

5.14 Option Byte Area (Customer Option)

The SC32L14T/14G has a separate Flash area for storing customer power-up initial settings. This area is called the option byte area (Customer Option). Users can configure Customer Option items through the host computer during programming. During the programming process, the configured values are written to the Customer Option area. During the reset initialization phase of the IC, the Customer Option data is used as the initial settings. You can also temporarily modify Customer Option items by manipulating the Customer Option mapping registers. However, please note that modifying the mapping registers only implements temporary adjustments and has no effect on the settings in the Customer Option area. After a chip reset, it will still be initialized according to the Customer Option parameters selected during programming.

The operation method of Customer Option related mapping registers is as follows:

Reading and writing Customer Option-related SFRs are controlled by the OPINX and OPREG registers. The specific location of each Customer Option SFR is determined by OPINX, as shown in the following table.

Register	Address	Description	Reset Value
OPINX	0x4000_03F8	Customer Option Pointer	0x0000_0000
OPREG	0x4000_03FC	Customer Option Register	0x0000_0000
COPT0_CFG	0XC1 @ OPINX	Customer Option Mapping Register0	0x0000_0000
COPT1_CFG	0XC2 @ OPINX	Customer Option Mapping Register1	0x0000_0000

5.14.1 Customer Option Map Register

Before using OPINX and OPREG to rewrite the IFB mapping register, you should first turn on the clock enable switch (AHB_CFG.IFBEN) of the Customer Option register:

5.14.1.1 AHB Bus peripheral clock enable register AHB_CFG

Register	R/W	Description	Reset Value
AHB_CFG	R/W	AHB Bus Peripheral Clock Enable Register	0x0020_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	CLKDIV[2:0]			-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	IFBEN	CRCEN	DMAEN

Bit number	Bit Mnemonic	Description
2	IFBEN	Customer Option Mapping Register Clock Enable Bit Before rewrite IFB mapping register by OPINX and OPREG,it is necessary to enable IFBEN. 0: Disable 1: Enable

5.14.1.2 Customer Option Map Register 0 COPT0_CFG

Register	R/W	Description	Reset Value
COPT0_CFG	R/W	Customer Option Mapping Register0	0x0000_0000

7	6	5	4	3	2	1	0
HIRC_SDIV[1:0]		-	-	-	DISLVR	LVRS[1:0]	

Bit number	Bit Mnemonic	Description
7~6	HIRC_SDIV[1:0]	HIRC frequency division selection bit 00: When SYSCLKSW=0, the system clock frequency is f_{HIRC}/2. 01: When SYSCLKSW=0, the system clock frequency is f_{HIRC}/2. 10: When SYSCLKSW=0, the system clock frequency is f_{HIRC}/4. 11: When SYSCLKSW=0, the system clock frequency is f_{HIRC}/8.
2	DISLVR	LVR Switch 0: LVR Enable 1: LVR Disable
1~0	LVRS[1:0]	LVR Voltage Select Control 11: 4.3V Reset 10: 3.7V Reset 01: 2.9V Reset 00: 1.7V Reset
5~3	-	Reserved

5.14.1.3 Customer Option Map Register 1 COPT1_CFG

Register	R/W	Description	Reset Value
COPT1_CFG	R/W	Customer Option Mapping Register1	0x0000_0000

7	6	5	4	3	2	1	0
ENWDT	DISJTG	DISRST	-	-	-	OP_BL[1:0]	

Bit number	Bit Mnemonic	Description
7	ENWDT	WDT Switch 0: WDT disable 1: WDT enable
6	DISJTG	JTAG Switch Control Bit 0: JTAG Mode Enable, corresponding pin can only work as T_CLK/T_DIO 1: Normal Mode Enable, JTAG function disable
5	DISRST	Reset Pin Switch Control Bit **This bit is read only.** 0: RST corresponding pin is used as reset pin 1: RST corresponding pin is used as normal GPIO pin
1~0	OP_BL[1:0]	Boot area selection after reset **This bit is read only.** 00: Boot from APROM after reset 01: Boot from LDROM after reset

Bit number	Bit Mnemonic	Description
		10: Boot from embedded SRAM after reset 11: Reserved
4~2	-	Reserved

6 Power, Reset And System Clock（RCC）

6.1 Power-on Reset

After the SC32L14T/14G power-on, the processes carried out before execution of client software are as follows:

① Reset stage
② Loading information stage
③ Normal operation stage

6.1.1 Reset Stage

The SC32L14T/14G will always be reset until the voltage supplied to SC32L14T/14G is higher than a certain voltage, and the internal Clock starts to be effective. The duration of reset stage is related to rising speed of external power. Once the external supply voltage is up to built-in POR voltage, the reset stage would be completed.

6.1.2 Loading Information Stage

There is a warm-up counter inside The SC32L14T/14G. During the reset stage, the warm-up counter is cleared to 0 until the voltage exceeds the POR voltage, the built-in HIRC oscillator starts to oscillate, and the warm-up counter starts counting. When the internal warm-up counter counts to a certain number, the IFB (including Customer Option) data in the Flash ROM will be periodically read into the system registers. Once all IFB data has been read, the Warm-up and Loading Information stage ends, and the system enters normal operation mode.

6.1.3 Normal Operation Stage

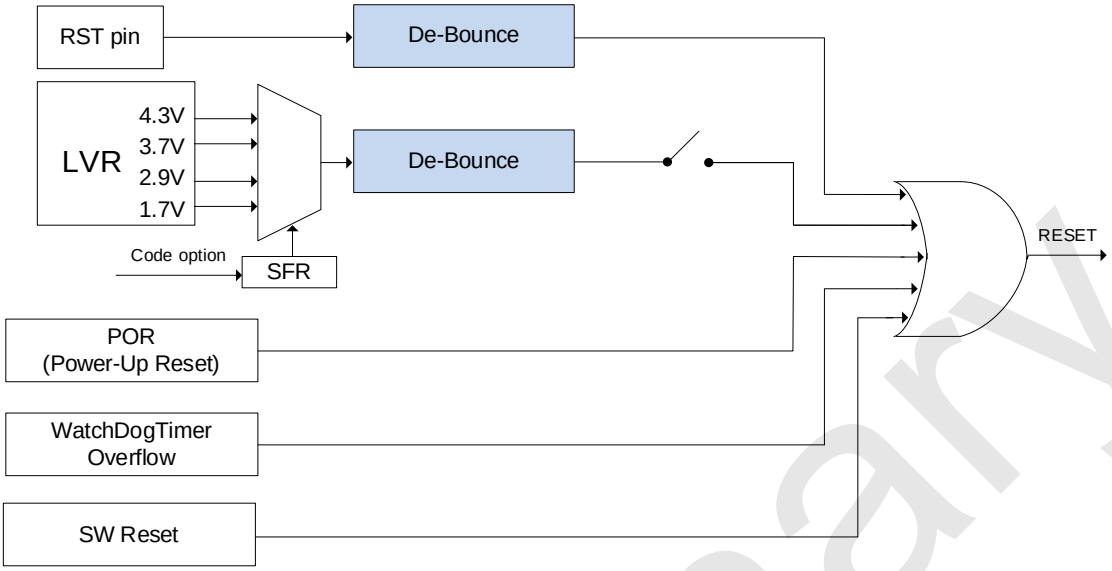
After finishing the Loading Information stage, The SC32L14T/14G starts to read the instruction code from Flash and enters the normal operation stage. The LVR voltage is the set value of Customer Option written by the user.

6.2 Reset Modes

The SC32L14T/14G has two types of resets: hardware reset and software reset. After a reset occurs, all registers will be restored to their reset values. The SC32L14T/14G has 5 reset methods, the first four are hardware reset:

- External reset
- Low-voltage reset LVR
- Power-on reset POR
- Watchdog WDT reset
- Software reset

The circuit diagram of the reset part of the SC32L14T/14G is as follows:



SC32L14T/14G Reset Circuit Diagram

6.2.1 Hardware reset

Hardware Reset can be performed in the following four ways：

① External RST reset

② Low voltage reset LVR

③ Power-on reset POR

④ Watchdog timer reset WDT

6.2.1.1 External RST reset

The SC32L14T/14G can achieve an external RST reset by inputting a low-level reset pulse signal with a pulse width greater than 18μs to the external RST pin.

User can configure the PE5/NRST pin as RST (reset pin) using the programming host software by Customer Option before programming

When this pin is configured as a reset pin, it cannot be used as a GPIO.

When this pin is configured as a GPIO pin, its reset function is unavailable.

6.2.1.2 Low voltage reset LVR

The SC32L14T/14G has a built-in low-voltage reset circuit that supports four threshold voltage options: 4.3V, 3.7V, 2.9V, and 1.7V. The factory default threshold voltage is 1.7V. Users can reconfigure this value by setting the Customer Option value during programming. When V_{DD} falls below the set threshold for a period exceeding the debounce time T_{LVR} of approximately 30μs, the chip will reset.

6.2.1.3 Power-on reset POR

The SC32L14T/14G has a power-on reset circuit inside. When the power supply voltage V_{DD} reaches the POR reset voltage, the system automatically resets.

6.2.1.4 Watchdog timer reset WDT

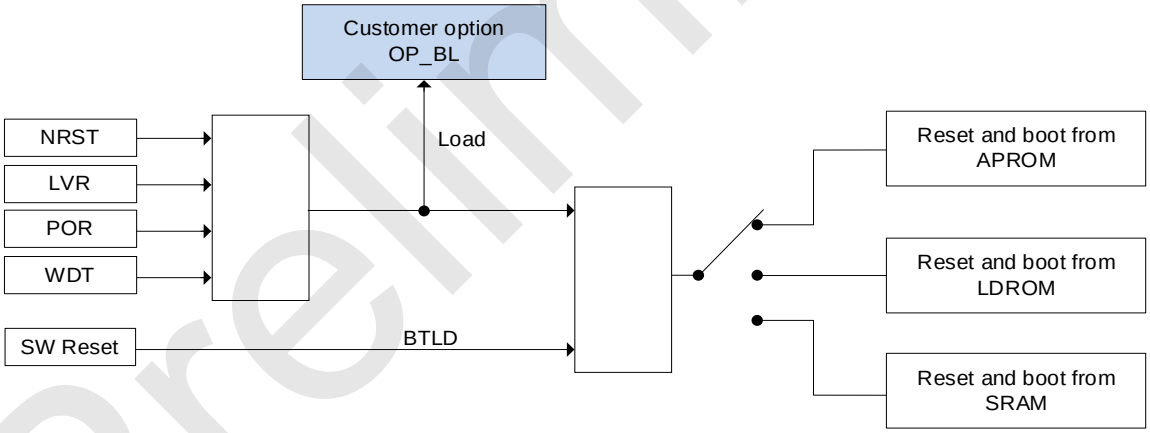
The SC32L14T/14G has a WDT, the clock source of which is the built-in 32 kHz oscillator. The user can choose whether to enable the watchdog reset function by Customer Option. A watchdog reset occurs when a watchdog event occurs.

6.2.2 Software reset

The SC32L14T/14G provides a software reset function. Enable RST(IAP_CON.8) will immediately reset the system.

6.2.3 Boot area after the reset

After hardware reset through external RST, low voltage reset (LVR), power-on reset (POR), or watchdog reset (WDT), the chip boots from the startup area (APROM / LDROM / SRAM) set by the user in OP_BL. After the software reset, the chip boots from the startup area (APROM / LDROM / SRAM) set by BTLD[1:0].



SC32L14T/14G Boot Area Switching diagram after reset

6.2.4 Initial Reset State

When SC32L14T/14G is in the reset state, most registers return to their initial state. The watchdog (WDT) is in the disabled state. 'Hot-start' resets (such as WDT, LVR, software reset, etc.) do not affect SRAM, and SRAM values remain the same as before the reset.

Note: Loss of SRAM content occurs when the power supply voltage drops to a level where RAM cannot retain data.

6.3 Clock

6.3.1 System Clock Source

Four different clock sources can be used to drive the system clock (SYSCLK):

- Built-in high-frequency 48MHz oscillator (HIRC)
- External high-frequency crystal oscillator (HXT)
- Built-in low-frequency 32kHz oscillator (LIRC)
- External low-frequency crystal oscillator (LXT)

Note：

1. **The default system clock source at power-up is HIRC, and it's frequency is f_{HIRC}/2. Users can switch the clock source through software during normal operation after power-up. Before switching, ensure that the selected clock source is in a stable operating state.**
2. **Regardless of the chosen clock source to switch to, the system clock source must first be switched to HIRC before transitioning to the target clock source.**

6.3.2 Built-in High-Frequency 48MHz Oscillator (HIRC)

The built-in high-frequency clock HIRC can be enabled by setting the HIRCEN position of the register RCC_CFG0 to 1, or cleared to 0 to disable. Additionally, the user must first write a value greater than 0x40 to the RCC protection register (RCC_KEY) before they can modify RCC_CFG0 and RCC_CFG1.

The HIRC has the following functions and features:

- Can be selected as the system operating clock
- Default system clock frequency when power on "f_{SYS}" is $f_{HIRC/2}$
- Frequency error: Within ±1% @ -40 ~ 105℃ @ 1.8V~ 5.5V
- The system clock can be automatically calibrated by 32.768 kHz external crystal oscillator, after calibration HIRC accuracy can be infinitely close to the accuracy of external 32.768 kHz crystal oscillator

6.3.3 Built-In High-Frequency Oscillator Circuit, Can Be Connected to an External 2~16MHz High-Frequency Oscillator (HXT)

The external high-frequency crystal oscillator (HXT) can be enabled by setting the HXTEN bit in the RCC_CFG0 register to 1, or disabled by clearing it to 0. Additionally, the user must first write a value greater than 0x40 to the RCC protection register (RCC_KEY) before they can modify RCC_CFG0 and RCC_CFG1.

Furthermore, the user needs to set the appropriate CRY_HF value based on the external high-frequency crystal oscillator frequency. When the external high-frequency crystal frequency is less than 12 MHz, CRY_HF should be written as 0; when the frequency is greater than 12 MHz, CRY_HF should be written as 1.

HXT has the following functions and features

- Can be selected as the system operating clock
- Can be externally connected to a 2~16MHz high-frequency oscillator

6.3.4 Built-in Low-Frequency 32kHz Oscillator (LIRC)

The built-in low-frequency clock (LIRC) can be enabled by setting the LIRCEN bit in the RCC_CFG0 register to 1, or disabled by clearing it to 0. Additionally, the user must first write a value greater than 0x40 to the RCC protection register (RCC_KEY) before they can modify RCC_CFG0 and RCC_CFG1.

LIRC has the following functions and features:

- Can be selected as the system operating clock
- Can be selected as the Base Timer clock source
- Fixed as the WDT clock source, this clock source must be enabled after WDT is enabled
- Frequency error: Within ±4% @ 25℃ @ 1.8V~ 5.5V, after register correction

6.3.5 Built-In Low-Frequency Oscillator Circuit, Can Be Connected to an External Low-Frequency Oscillator Circuit (LXT)

The built-in low-frequency clock (LXT) can be enabled by setting the LXTEN bit in the RCC_CFG0 register to 1, or disabled by clearing it to 0. Additionally, the user must first write a value greater than 0x40 to the RCC protection register (RCC_KEY) before they can modify RCC_CFG0 and RCC_CFG1.

LXT has the following functions and features:

- Can be selected as the system operating clock
- Can be selected as the Base Timer clock source
- External 32.768kHz low-frequency oscillator
- Can automatically calibrate HIRC via LXT

6.4 Register Access Clock and Peripheral Clock Sources

6.4.1 Register Access Clock

The register access clock is the clock signal that drives the Cortex ® -M0+ core and internal bus operations. This signal directly drives the instruction execution pipeline, register group access, and data transmission between the core and the bus.

Register access clocks are strictly synchronized with the AHB (Advanced High-performance Bus) and APB (Advanced Peripheral Bus) bus clocks, ensuring that CPU core operations and peripheral interfaces work together within a unified timing framework. Users must enable the bus clock and gate the peripheral clocks using the AHB bus peripheral clock enable register (AHB_CFG) or the APB bus peripheral clock enable register (APBn_CFG, n=0-2). Read and write operations to peripheral registers are only possible when both the bus and register access clock bits for the corresponding peripheral are enabled; otherwise, the hardware protection mechanism will be triggered, rendering the access invalid.

6.4.2 Peripheral Clock Source

The peripheral clock source provides independent clock signals for specific peripheral modules (such as

PWM, UART, ADC, etc.). It can be frequency-divided/multiplied products of the system clock or independent built-in or external clock sources (such as internal RC oscillators, external crystals, etc.). The presence of peripheral clock sources allows different peripherals to select the optimal clock frequency and stability based on their requirements. Users can also reduce power consumption by individually turning off the clocks of unused peripherals.

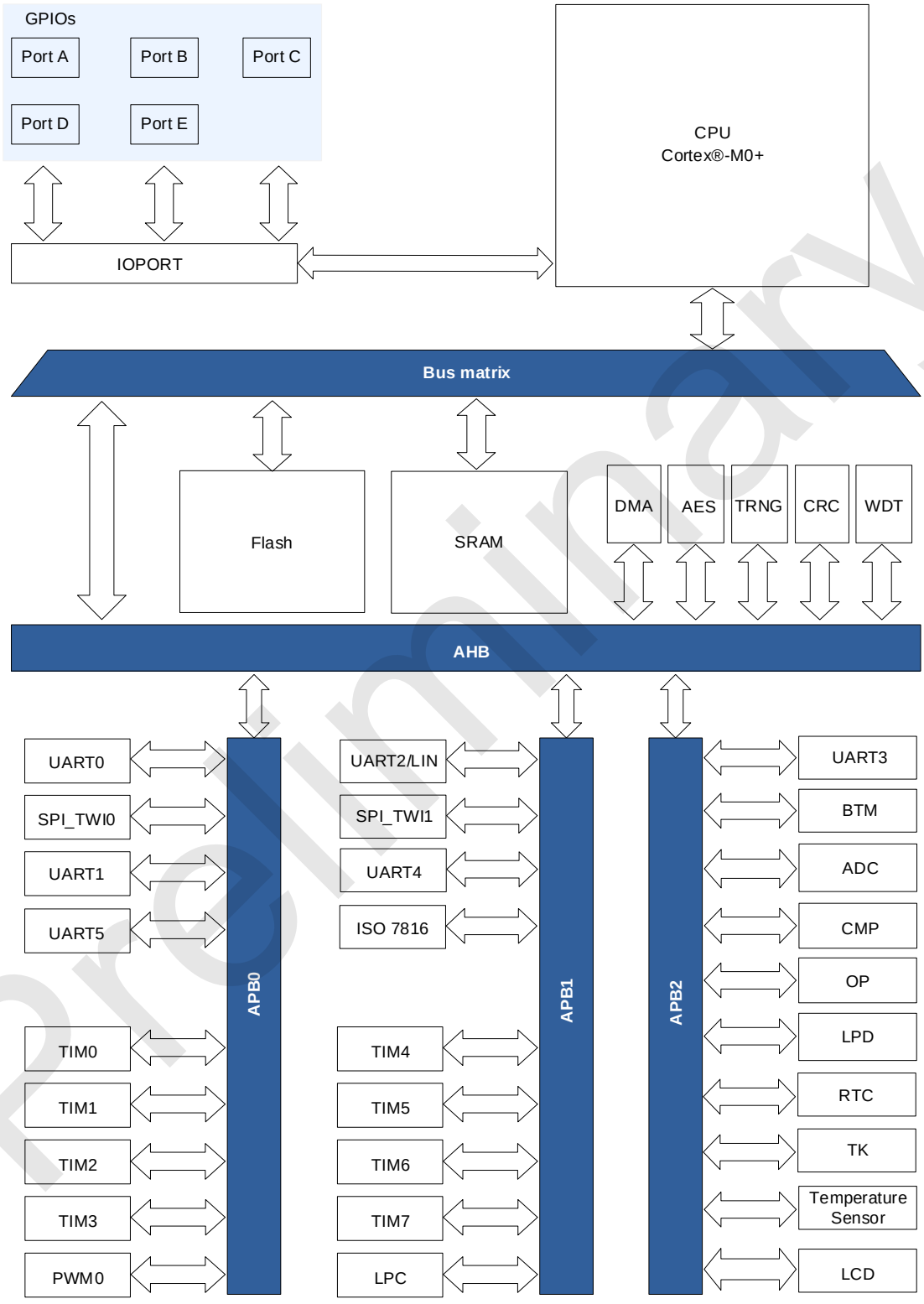
Some peripherals of the SC32L14T/14G offer multiple optional clock sources. Users can select the appropriate clock source for the peripherals through the peripheral clock source selection register (RCC_CFGn, n=0~1).

6.4.3 Bus Clock

Users can configure the frequencies of the IOPORT, AHB, APB0, APB1, and APB2 domains through multiple prescalers.

- IOPORT: The main clock of the GPIO domain, derived by dividing the system clock (SYSCLK), with a maximum frequency of 48MHz, all GPIOs are driven by IOPORT.
- HCLK: The main clock of the AHB domain, derived by dividing the system clock (SYSCLK), with a maximum frequency of 48MHz. It drives components such as the Cortex®-M0+ core, memory, and DMA.
- PCLK0: The main clock of the APB0 domain, derived by dividing HCLK, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB0 bus are driven by PCLK0.
- PCLK1: The main clock of the APB1 domain, derived by dividing HCLK, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB1 bus are driven by PCLK1.
- PCLK2: The main clock of the APB2 domain, derived by dividing HCLK, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB2 bus are driven by PCLK2.

The bus architecture diagram is shown below. The frequency at which peripheral registers are read depends on the bus frequency to which the peripheral is connected.



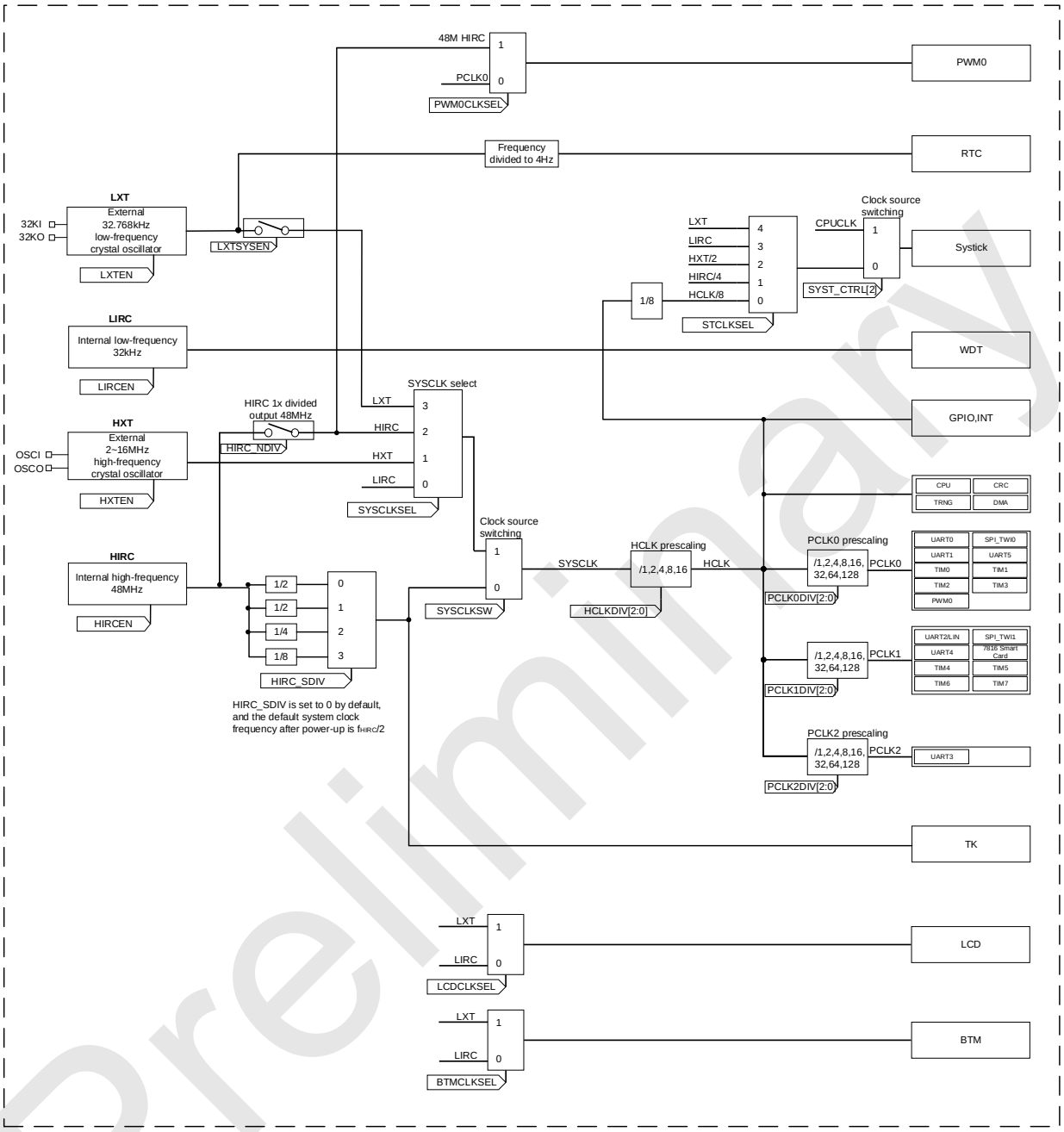
Bus architecture diagram

6.4.4 Peripheral Clock

The clocks of bus-carried peripherals are generally provided by their corresponding bus clocks, but the following peripherals can be clocked by other clock sources:

- RTC uses LXT divided to 4Hz as the RTC clock frequency
- TK uses the divided frequency of HIRC selected by HIRC_SDIV as the TK clock frequency
- PWM0 has the following clock sources to choose from:
  - PCLK0, the clock on the bus where PWM0 is located
  - 48M HIRC, the clock derived from the 1x divided HIRC
- LCD has the following clock sources to choose from:
  - LIRC, internal low-frequency clock
  - LXT, the external low-frequency crystal oscillator clock
- BTM has the following clock sources to choose from:
  - LIRC, internal low-frequency clock
  - LXT, the external low-frequency crystal oscillator clock
- The WDT clock source is fixed to LIRC. When WDT is enabled, LIRC will automatically turn on. During WDT operation, LIRC always keeps oscillating and cannot be turned off by the user.
- SysTick has the following clock sources to choose from:
  - LXT, the external low-frequency crystal oscillator clock
  - LIRC, internal low-frequency clock
  - HXT/2, the external high-frequency crystal oscillator clock divided by 2
  - HIRC/4, the internal high-frequency clock divided by 4
  - HCLK/8, the AHB bus clock divided by 8
  - CPUCLK, the core clock

6.4.5 Peripheral Clock Block Diagram



Note: After system power-up, the default clock frequency f_{SYS} is $f_{HIRC}/2$. The user can select the desired clock source by modifying the register bits SYSCLKSW and SYSCLKSEL.

6.4.6 Peripheral Clock Enable Register

Each peripheral clock can be enabled through the corresponding enable bits in the AHB_CFG and APBn_CFG registers. When the peripheral clock is not activated, the peripheral registers cannot be accessed for read/write operations.

6.4.7 Low Power Mode Clock

In the low-power STOP mode, the CPU clock and most clock sources, including peripheral clocks, will stop, and the program execution will halt. However, the following clock sources continue to work in low-power

mode:

- The built-in low-frequency clock LIRC
- The external low-frequency oscillator clock LXT

7 Interrupts

- M0+ core could provide a maximum of 32 interrupt sources, numbered from 0 to 31, while SC32L14T/14G series has 27 interrupt sources
- Four-level interrupt priorities can be configured (core feature), and the interrupt priorities are set through the Interrupt Priority Registers in the core registers

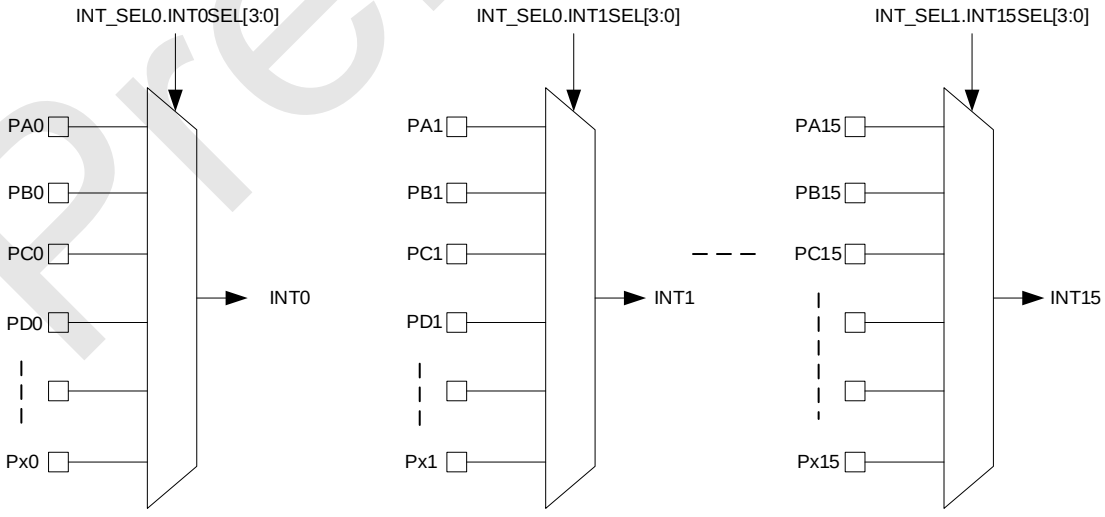
7.1 External interrupts INT0~15

External interrupts comprise 16 interrupt sources, occupying a total of 4 interrupt vectors. All 16 external interrupt sources can be configured to respond to rising edges, falling edges, or both edges. Once configured, these interrupts can cover all GPIO pins. When the corresponding event occurs, software sets the corresponding interrupt flag (RIF/FIF to 1), triggering entry into the corresponding interrupt service.

The external interrupt features of the SC32L14T/14G series are as follows:

- 16 INT interrupt sources, occupying 4 interrupt vectors in total
- After configuration, INT can cover all GPIO pins
- All INT sources can be configured for rising edge, falling edge, or both edge interrupts, each having independent corresponding interrupt flag
- Software sets the corresponding interrupt flag can trigger entry into the corresponding interrupt service

Note: When using INT functions, users need to manually set the GPIO port corresponding to INTn (n=0~15) to pull-up input mode. External interrupts cannot be detected in output mode.



External Interrupt Port Multiplexer

7.2 Interrupt and Events

- When NVIC is disabled, interrupt request masks are enabled, events can be generated, but interrupt cannot be generated
- When NVIC is enabled, interrupt request masks act as internal master interrupt control bit in the module

7.3 Interrupt Source and Vector

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
0	**-**	-	0x0000_0000	**-**		-	\	\	YES
1	**-**	Fixed	0x0000_0004	**RESET**	PRIMASK	SCB	\	\	YES
2	**-**	Fixed	0x0000_0008	**NMI_Handler**		SCB	\	\	YES
3	**-**	Fixed	0x0000_000C	**HardFault_Handler**	PRIMASK	SCB	\	\	YES
4~10	**-**	-	0x0000_0010 - 0x0000_0028	**-**		-	\	\	YES
11	**-**	Settable		**SVC_Handler**	PRIMASK	SCB	\	\	YES
12~13	**-**	-	0x0000_0030 0x0000_0034	**-**		-	\	\	YES
14	**-**	Settable	0x0000_0038	**PendSV_Handler**	PRIMASK	SCB	\	\	YES
15	**-**	Settable	0x0000_003C	**SysTick_Handler**	PRIMASK	SysTick_CTRL	\	\	NO
16	**0**	Settable	0x0000_0040	**INT0**	NVIC->ISER[0].0	INTF_IE->ENFx, x=0 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
17	**1**	Settable	0x0000_0044	**INT1-7**	NVIC->ISER[0].1	INTF_IE->ENFx, x=1~7 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
18	**2**	Settable	0x0000_0048	**INT8-11**	NVIC->ISER[0].2	INTF_IE->ENFx, x=8~11 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
19	**3**	Settable	0x0000_004C	**INT12-15**	NVIC->ISER[0].3	INTF_IE->ENFx, x=12~15 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
20	**4**	Settable	0x0000_0050	**RCC** Stop Oscillation Detection	NVIC->ISER[0].4	RCC_CFG->INTEN	\	RCC_STS->CLKFIF	NO
21	**5**	Settable	0x0000_0054	**LPD**	NVIC->ISER[0].5	LPD_IDE->INTEN	\	LPD_CON->LPDIF	NO
22	**6**	Settable	0x0000_0058	**BTM**	NVIC->ISER[0].6	BTM_CON->INTEN	\	BTM_STS->BTMIF	YES

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
23	7	Settable	0x0000_005C	**UART0**	NVIC->ISER[0].7	UART0_IDE->INTEN	UART0_IDE->TXIE UART0_IDE->RXIE	UART0_STS->TXIF UART0_STS->RXIF	YES
				UART2/LIN	\	UART2_IDE->INTEN	UART2_IDE->TXIE UART2_IDE->RXIE UART2_IDE->BKIE UART2_IDE->SLVHEIE	UART2_STS->TXIF UART2_STS->RXIF UART2_STS->BKIF UART2_STS->SLVHEIF	YES
				UART4	\	UART4_IDE->INTEN	UART4_IDE->TXIE UART4_IDE->RXIE	UART4_STS->TXIF UART4_STS->RXIF	YES
24	8	Settable	0x0000_0060	**UART1**	NVIC->ISER[0].8	UART1_IDE->INTEN	UART1_IDE->TXIE UART1_IDE->RXIE	UART1_STS->TXIF UART1_STS->RXIF	YES
				UART3	\	UART3_IDE->INTEN	UART3_IDE->TXIE UART3_IDE->RXIE	UART3_STS->TXIF UART3_STS->RXIF	YES
				UART5	\	UART5_IDE->INTEN	UART5_IDE->TXIE UART5_IDE->RXIE	UART5_STS->TXIF UART5_STS->RXIF	YES
				7816 SMCI	\	SC0_IDE->INTEN	SC0_IDE->TXIE SC0_IDE->RXIE SC0_IDE->ERRIE	SC0_STS->TC SC0_STS->RC SC0_STS->ROVF SC0_STS->FER SC0_STS->WTER SC0_STS->RPER SC0_STS->TPER	NO
25	9	Settable	0x0000_0064	**SPI0/TWI0**	NVIC->ISER[0].9	TWI_SPI0_IDE->INTEN	TWI_SPI0_IDE->TBIE	TWI_SPI0_STS->QTWIF TWI_SPI0_STS->TXEIF	NO
26	10	Settable	0x0000_0068	**SPI1/TWI1**	NVIC->ISER[0].10	TWI_SPI1_IDE->INTEN	TWI_SPI1_IDE->TBIE	TWI_SPI1_STS->QTWIF TWI_SPI1_STS->TXEIF	NO
27	11	Settable	0x0000_006C	**DMA0**	NVIC->ISER[0].11	DMA0_CFG->INTEN	DMA0_CFG->TCIE DMA0_CFG->HTIE DMA0_CFG->TEIE	DMA0_STS->GIF DMA0_STS->TCIF DMA0_STS->HTIF DMA0_STS->TEIF	NO
28	12	Settable	0x0000_0070	**DMA1**	NVIC->ISER[0].12	DMA1_CFG->INTEN	DMA1_CFG->TCIE DMA1_CFG->HTIE DMA1_CFG->TEIE	DMA1_STS->GIF DMA1_STS->TCIF DMA1_STS->HTIF DMA1_STS->TEIF	NO
29	13	Reserved	0x0000_0074	\	NVIC->ISER[0].13	\	\	\	
30	14	Reserved	0x0000_0078	\	NVIC->ISER[0].14	\	\	\	

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
31	15	Settable	0x0000_007C	**TIM0**	NVIC->ISER[0].15	TIM0_IDE->INTEN	TIM0_IDE->TIE TIM0_IDE->EXFIE TIM0_IDE->EXRIE	TIM0_STS->TIF TIM0_STS->EXIF TIM0_STS->EXIR	NO
32	16	Settable	0x0000_0080	**TIM1**	NVIC->ISER[0].16	TIM1_IDE->INTEN	TIM1_IDE->TIE TIM1_IDE->EXFIE TIM1_IDE->EXRIE	TIM1_STS->TIF TIM1_STS->EXIF TIM1_STS->EXIR	NO
33	17	Settable	0x0000_0084	**TIM2**	NVIC->ISER[0].17	TIM2_IDE->INTEN	TIM2_IDE->TIE TIM2_IDE->EXFIE TIM2_IDE->EXRIE	TIM2_STS->TIF TIM2_STS->EXIF TIM2_STS->EXIR	NO
34	18	Settable	0x0000_0088	**TIM3**	NVIC->ISER[0].18	TIM3_IDE->INTEN	TIM3_IDE->TIE TIM3_IDE->EXFIE TIM3_IDE->EXRIE	TIM3_STS->TIF TIM3_STS->EXIF TIM3_STS->EXIR	NO
35	19	Settable	0x0000_008C	**TIM4**	NVIC->ISER[0].19	TIM4_IDE->INTEN	TIM4_IDE->TIE TIM4_IDE->EXFIE TIM4_IDE->EXRIE	TIM4_STS->TIF TIM4_STS->EXIF TIM4_STS->EXIR	NO
				TIM5	\	TIM5_IDE->INTEN	TIM5_IDE->TIE TIM5_IDE->EXFIE TIM5_IDE->EXRIE	TIM5_STS->TIF TIM5_STS->EXIF TIM5_STS->EXIR	NO
36	20	Settable	0x0000_0090	**TIM6**	NVIC->ISER[0].20	TIM6_IDE->INTEN	TIM6_IDE->TIE TIM6_IDE->EXFIE TIM6_IDE->EXRIE	TIM6_STS->TIF TIM6_STS->EXIF TIM6_STS->EXIR	NO
				TIM7	\	TIM7_IDE->INTEN	TIM7_IDE->TIE TIM7_IDE->EXFIE TIM7_IDE->EXRIE	TIM7_STS->TIF TIM7_STS->EXIF TIM7_STS->EXIR	NO
37	21	Settable	0x0000_0094	**PWM0**	NVIC->ISER[0].21	PWM0_CON->INTEN	\	PWM0_STS->PWMIF	NO
38	22	Reserved	0x0000_0098	\	NVIC->ISER[0].22	\	\	\	
39	23	Settable	0x0000_009C	**TRNG**	NVIC->ISER[0].23	SUB_CFG->TINTEN	SUB_CFG->DRDYIE	TRNG_STS->SEIS TRNG_STS->DRDYIF	NO
40	24	Settable	0x0000_00A0	**AES**	NVIC->ISER[0].24	\	SUB_CFG->CCFIE	AES_STS->CCFIF	NO
41	25	Settable	0x0000_00A4	**RTC**	NVIC->ISER[0].25	RTC_CON->INTEN	RTC_CON->WALIE RTC_CON->CT[2:0]	RTC_STS->WALIF RTC_STS->RTCCTIF	YES
42	26	Settable	0x0000_00A8	**LPC**	NVIC->ISER[0].26	LPC_IDE->INTEN	LPC_IDE->DIRIE LPC_IDE->CAIE LPC_IDE->CBIE LPC_IDE->RFAIE LPC_IDE->RFBIE	LPC_STS->DIRIF LPC_STS->CAIF LPC_STS->CBIF LPC_STS->RFAIF LPC_STS->RFBIF	YES
43	27	Reserved	0x0000_00AC	\	\	\	\	\	

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
44	**28**	Reserved	0x0000_00B0	\	\	\	\	\	
45	**29**	Settable	0x0000_00B4	**ADC**	NVIC->ISER[0].29	ADC_CON->INTEN	\	ADC_STS->ADCIF	NO
46	**30**	Settable	0x0000_00B8	**CMP**	NVIC->ISER[0].30	CMP_CFG->CMPIM[1:0]	\	CMP_STS->CMPIF	YES
47	**31**	Settable	0x0000_00BC	**TK**	NVIC->ISER[0].31	TKCON->INTEN	\	TKCON->TKIF	YES

8 Power Saving Mode

Upon initial power-up, the system runs in Operation Mode. Additionally, three power-saving modes are available:

- Low-Speed Mode: The system clock source can be LIRC, and the CPU can operate at 32kHz
- IDLE Mode: The system can be awakened by any interrupt
- STOP Mode: The system can be awakened by INT0~15, Base Timer, TK, UART0~5, RTC, LPC and CMP

9 Low Voltage Detector (LPD)

9.1 Overview

The SC32L14T/14G has a built-in low-voltage detector (LPD) circuit that monitors the supply voltage V_{DD} and compares it with the LPD threshold voltage V_{LPD}.

When the V_{DD} voltage drops below V_{LPD} or rises above V_{LPD}, the LPD status flag (LPDOF) will change accordingly, and the LPD interrupt flag (LPDIF) will be set. If the LPD interrupt is enabled, an LPD interrupt will be triggered. The status flag LPDOF is automatically set and cleared by hardware, while the interrupt flag LPDIF must be cleared by software.

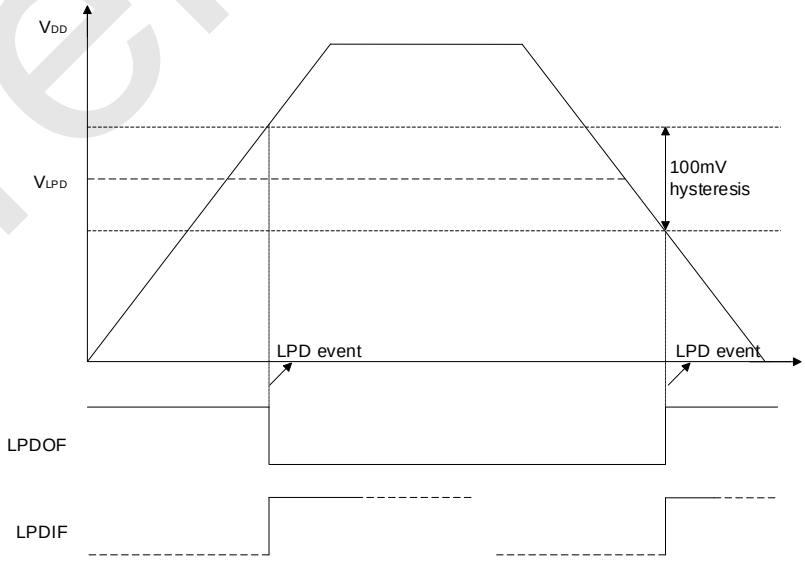
The LPD threshold voltage of the SC32L14T/14G ranges from 1.85V to 3.25V, divided into 8 levels with a 200mV step size. Users can read the LPD status, obtain the LPD interrupt flag, and configure the LPD threshold voltage level through the LPD_CON register

Note: In STOP mode, the LPD power supply is turned off.

9.2 Hysteresis Function

The LPD has a hysteresis function that enhances the chip's anti-interference capability. The threshold voltage V_{LPD} has a threshold range of approximately 100mV. The interrupt flag LPDIF is set only when the power supply voltage V_{DD} exceeds the maximum threshold range or falls below the minimum threshold range.

The LPD threshold diagram is as follows:



The LPD threshold diagram

10 GPIO

10.1 Clock Source

M0+ core can achieve single-cycle access to GPIO through the IOPORT bus, resulting in highly efficient data transfer. The IOPORT bus clock is derived from HCLK.

10.2 Feature

The GPIO port features of the SC32L14T/14G are as follows:

- A maximum of 77 bidirectional independently controlled GPIOs
- CPU can access GPIO ports through the IOPORT bus in a single cycle
- Independent setting of pull-up resistors
- All ports have four levels of source driving capability
- All I/Os have high sink current driving capability (50mA)
- 16 I/Os in one group
- Whether input mode or output mode, reading from the port data register retrieves the actual status value of the port

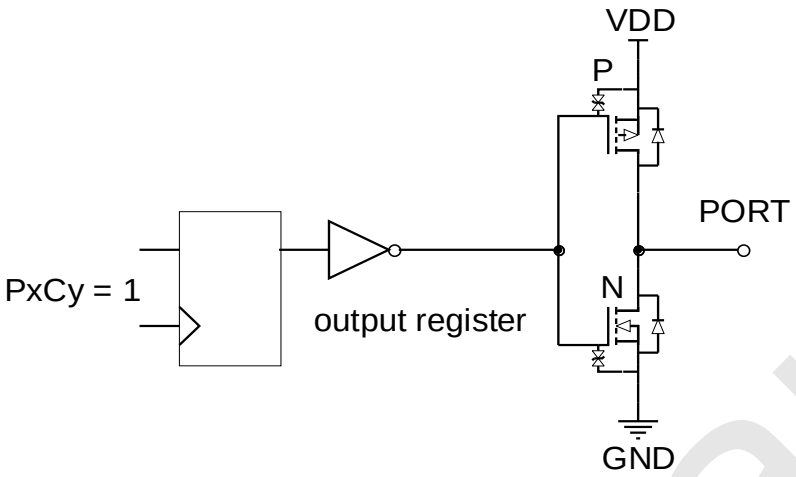
Note: Unused and non-exported ports should be set to strong push-pull output mode

10.3 GPIO Structure Diagram

10.3.1 Strong Push-pull Output Mode

In the strong push-pull output mode, it can provide continuous high-current drive: For detailed electrical parameters, please refer to the "GPIO Parameters" section.

The schematic diagram of the port structure of the strong push-pull output mode is as follows:

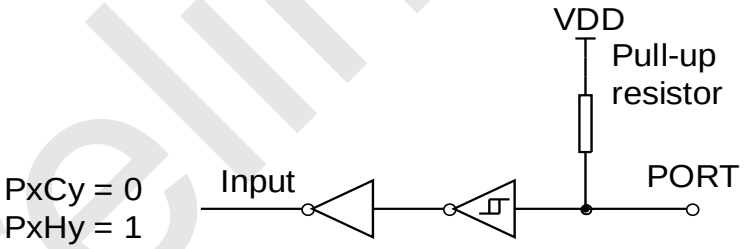


Strong push-pull output mode

10.3.2 Pull-up Input Mode

In the pull-up input mode, a pull-up resistor is constantly connected to the input port. Only when the input port is pulled low, the low-level signal is detected.

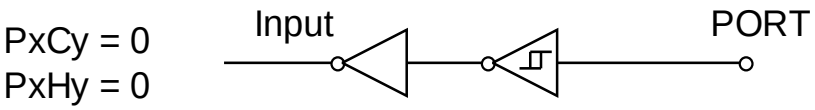
The schematic diagram of the port structure with pull-up input mode is as follows:



Input mode with pull-up resistor

10.3.3 High Impedance Input Mode (Input only)

The schematic diagram of the port structure of the high impedance input mode is as follows:



High impedance input mode

11 Analog-to-Digital Converter ADC

11.1 Clock source

- The SC32L14T/14G ADC has only one clock source, which is derived from PCLK
- Conversion time is about 950ns

11.2 Feature

- Precision：14 bits
- Maximum Channels: Supports up to 23 channels:
  - 20 external ADC sampling channels and other functions multiplexed with I/O ports
  - 1 internal ADC channel can directly measure the V_{DD} voltage
  - 1 internal ADC channel can directly measure the OP output
  - One internal temperature sampling channel
- Built-in Reference Voltages: 2.4V, 2.048V, and 1.024V
- Reference Voltage Selection: V_{DD}, 2.4V, 2.048V and 1.024V
- ADC Input Channel Selection:
  - Can be configured through the ADCIS[4:0] bits
- Software-Triggered Conversion: The conversion process can be initiated by software
- Interrupt Support: Configurable ADC conversion completion interrupt
- Conversion Time: Sampling to completion time as low as 2μs
- DMA Transfer Support: ADC conversion completion can generate a DMA request
- Single-Channel Continuous Conversion Mode Support: Allows continuous conversion in single-channel mode
- Overflow Flag: The ADC conversion result supports an overflow flag, and the OVERRUN flag is in the same register (ADCV), allowing the user to read both at once

11.3 ADC Conversion Steps

The actual operation steps required for the user to perform ADC conversion are as follows:

① Set the ADC input pin; (set the bit corresponding to AINx as ADC input, usually the ADC pin will be fixed in advance);
② Set ADC reference voltage Vref, set the frequency used for ADC conversion.
③ Set ADCEN to enable the ADC module power supply.
④ Select ADC input channel; (set ADCIS bit, select ADC input channel).
⑤ Start ADCS and start conversion.
⑥ Wait for ADCIF=1. If the ADC interrupt is enabled, the ADC interrupt will be generated. The user needs to clear the EOC/ADCIF flag by software.
⑦ Get 14-bit data from ADCV, then one conversion is completed.
⑧ If the input channel is not changed, continuous conversion mode can be set by setting CONT to 1

through software. The conversion will continue until this bit is cleared to 0.

⑨ When the ADC conversion result overflows, the OVERRUN flag will set to 1.

⑩ Conversion data can be transferred using DMA.

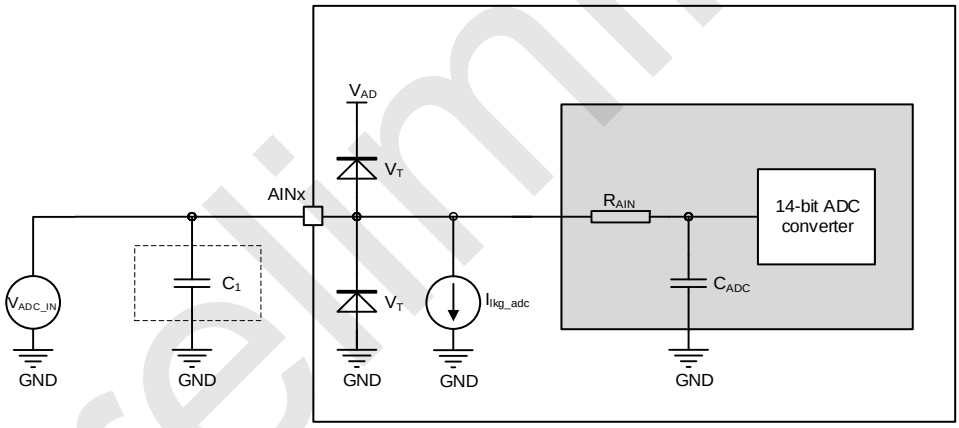
Note: Before setting the ADC_CON[8] bit, it is recommended that users first clear the ADCIF using software. Additionally, after the ADC interrupt service routine has been executed, the ADCIF should also be cleared to prevent continuous generation of ADC interrupts.

11.4 ADC Interrupt

After the SC32L14T/14G series ADC conversion complete, the ADCIF flag will be set, and if ADC_CON.INTEN=1, an interrupt will be generated.

Interrupt Event	Event Flag	Interrupt Enable Control Bit
ADC conversion completion interrupt request	ADCIF	ADC_CON->INTEN

11.5 ADC Structure Diagram



Note:

1. **C1 is an external 0.01μF capacitor. Users are advised to add this capacitor to improve the performance of the ADC.**
2. **For detailed electrical parameters related to the ADC, please refer to Section 32.10 ADC Characteristics.**

12 Temperature Sensor

12.1 Overview

The SC32L14T/14G series features a temperature sensor, and temperature sensor voltage can be measured though ADC.

12.2 Temperature Sensor Operation Steps

When using the temperature sensor, the ADC reference voltage should be set to the internal 2.4V reference. For every 1°C increase in temperature, the ADC conversion value will increase by a fixed amount. SinOne has pre-programmed the ADC conversion result corresponding to 25°C for each chip into a specific address during production.

The steps for operating the temperature sensor are as follows:

① Set the ADC reference voltage (Vref) to the internal 2.4V reference source and configure the ADC sampling period. It is recommended to select a sampling clock of 60 or more cycles. Then, enable the ADC module power.

② Select the ADC input channel as the temperature sensor channel.

③ Enable the temperature sensor by setting TS_EN to 1.

④ Wait for a delay of 20μs.

⑤ Set TS_CHOP to 0 to initiate the first ADC conversion. Once the conversion is complete, record the conversion value as ADC_{Value1}.

⑥ Set TS_CHOP to 1 to initiate the second ADC conversion. Once the conversion is complete, record the conversion value as ADC_{Value2}.

⑦ Calculate the average of the two conversion values：

$$ADC_{Value} = \frac{(ADC_{Value1} + ADC_{Value2})}{2}$$

⑧ Read the factory-programmed ADC conversion value for 25°C ($ADC_{ValueTest}$) from the corresponding address.

⑨ Substitute the values into the formula to calculate the current temperature:

$$Temperature = 25℃ + \frac{(ADC_{Value} - ADC_{ValueTest})}{33}$$

For more information about the temperature sensor, please refer to the “SinOne SC32L14T/14G Series MCU Application Guide”

13 Operational Amplifier (OP)

13.1 Overview

A built-in internal operational amplifier and programmable gain amplifier, offering a rail-to-rail input stage. The OP can be configured in PGA mode, featuring 5 non-inverting input terminals, 2 inverting input terminals, and 3 output terminals. It provides options for 8/16/32/64 times non-inverting gain and 7/15/31/63 times inverting gain.

13.2 Feature

A built-in variable gain amplifier, the characteristics of this OP are as follows:

- A rail-to-rail input stage
- Can be configurable as a Programmable Gain Amplifier (PGA)
  - Non-inverting gain: 8/16/32/64
  - Inverting gain: 7/15/31/63
- Two external pins for the non-inverting input: OP_P0 or OP_P1
- One external pin for the inverting input: OP_N
- One external pin for the output: OP_O
- The output can be directly connected to the ADC input
- The output can be directly connected to the positive input of a Comparator (CMP)
- Precision adjustment can be achieved by setting the PGA input offset control bit PGAOFC to 1, which will short the non-inverting and inverting input terminals of the OP (operational amplifier) module

13.3 OP Port Selection

13.3.1 OP Accuracy Adjustment

The accuracy of OP1/2 can be adjusted by enabling the PGA offset adjustment control bit (PGAOFC=1). This is achieved by shorting the non-inverting and inverting input terminals of the OP module internally. In other cases, PGAOFC is set to 0.

13.3.2 OP Non-inverting Input Selection

The non-inverting input terminal of OP module can be switched and selected by OPPSEL[2:0], and it has five options:

- OP_P0 external pin
- OP_P1 external pin
- Internal VSS
- Internal 1.2V reference
- V_{DD}

13.3.3 OP Inverting Input Selection

The inverting input terminal of the OP module has two options:

- OP_N external pin.

When choosing the OP_N external pin as the negative input for the OP, the OP input control bit OPNSEL should be set to 0, and the feedback resistor selection bits FDBRSEL[1:0] should be set to 01.

- Internal feedback resistor.

When choosing the internal feedback resistor as the negative input for the OP, the OP input control bit OPNSEL should be set to 1, and the feedback resistor selection bits FDBRSEL[1:0] should be set to 00, 11, or 10, and the internal gain can be selected by internal gain selection bits PGAGAN[1:0].

13.3.4 OP Output Selection

The output of the OP module has three options:

- Sampling channel of the AD converter

When OP output is used as an ADC input, users should set ENOP=1 to enable the OP module, then set ADCEN=1 to power on the ADC. The conversion result of OP can be directly obtained in the ADCV register by selecting the OP output port as the ADC input port through ADCIS[4:0].

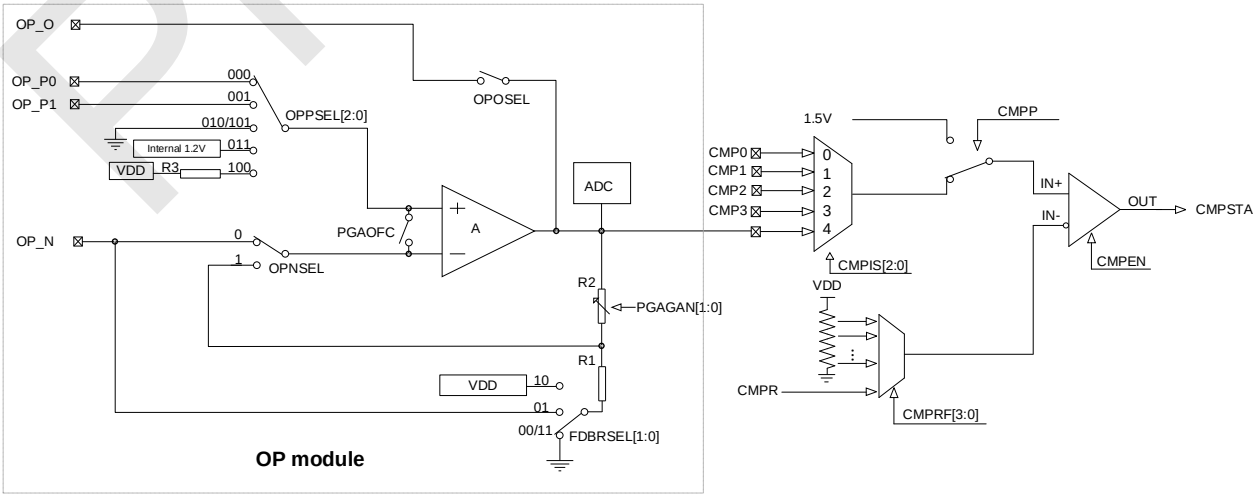
- Positive input of the CMP

When OP is used as the positive input of the CMP, users should set ENOP=1 to enable the OP module, then select OP output port as the CMP input port by channel control bit CMPIS[2:0].

- OP_O pin.

When OP outputs through the OP_O pin, users should set ENOP=1 to enable the OP module, then set OPOSEL=1.

13.4 OP Circuit Structure Diagram



14 Analog Comparator CMP

The SC32L14T/14G features a built-in analog comparator (CMP), and CMP interrupt can wake up the STOP Mode. It can be used for applications such as alarm circuits, power supply voltage monitoring circuits, zero-crossing detection circuits, etc.

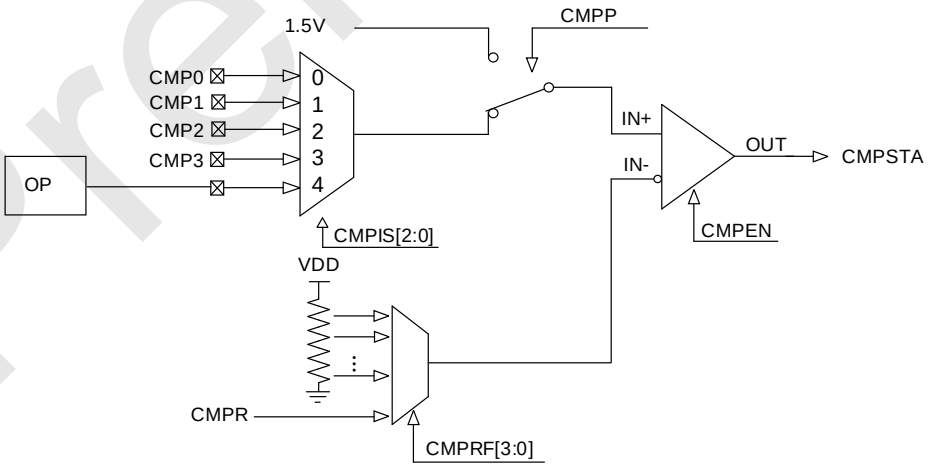
The comparator has five analog signal positive input terminals: CMP0~3 and OP output port, which can be selected through CMPIS [2:0]. The negative input terminal voltage can be switched through CMPRF[3:0] to an external voltage on the CMPR pin or one of the 15 reference voltages internally.

The interrupt mode of the comparator can be conveniently set using CMPIM[1:0]. When the interrupt condition set by CMPIM[1:0] occurs, the comparator interrupt flag CMPIF will set to 1. This interrupt flag needs to be cleared by software.

14.1 Feature

- Positive input has five options:
  - Four analog signal positive input terminals: CMP0~CMP3
  - OP output
- Negative input voltage can be selected from CMPR handover or one of the 15 comparison voltages derived from the internal V_{DD} division
- CMP interrupt can wake up the STOP Mode

14.2 Analog Comparator Structure Diagram



Analog Comparator Structure Diagram

15 AES hardware accelerator (AES)

15.1 Overview

The SC32L14T/14G series integrates an AES module, which supports data encryption and decryption. Multiple chaining modes are supported (ECB, CBC, CTR), for key size of 128/192/256 bits.

15.2 Clock source

The SC32L14T/14G AES clock source is derived from the HCLK.

15.3 Feature

- 128-bit data block processing
- Support for cipher key length of 128/192/256 bits
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB)
  - Cipher block chaining (CBC)
  - Counter (CTR)

16 True random number generator (TRNG)

16.1 Overview

The SC32L14T/14G series integrates a TRNG that can generate 32-bit true random numbers. Random numbers are generated from the input clock through an analog entropy source.

The TRNG generator has been tested using the German BSI AIS-31 statistical test (T0 to T8).

16.2 Clock source

The SC32L14T/14G TRNG has only one clock source, which is derived from HCLK.

16.3 Feature

- The RNG delivers 32-bit true random numbers
- If the randomness is low a seed error interrupt can be triggered
- An interrupt is generated when a random number is ready

17 UART0~5

17.1 Clock Source

The SC32L14T/14G UART has only one clock source, which is derived from PCLK.

17.2 Feature

- Six UARTs，UART0~5
- UART2 has a complete LIN interface
  - Can switch between master and slave modes
  - Supports hardware break sending in master mode (10/13 bits)
  - Supports hardware break detection in slave mode (10/11 bits)
  - Supports baud rate synchronization in slave mode
  - Provides related interrupts/status bits/flags/fault tolerance range
- UART0~5 ports can be mapped to 2 sets of IO pins
- Independent baud rate generator
- Each UART has four communication modes to choose from:
  - Mode 0: 8-bit half-duplex synchronous communication mode, serial data is transmitted and received on the RX pin. The TX pin is used as the transmit shift clock. Each frame transmits or receives 8 bits, with the low bit transmitted or received first
  - Mode 1: 10-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, and 1 stop bit. The communication baud rate is variable
  - Mode 2: Reserved
  - Mode 3: 11-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, 1 programmable 9th bit and 1 stop bit. The communication baud rate is variable
- Interrupts will be generated and corresponding flags TXIF and RXIF will be set when transmission and reception are complete. Interrupt flags need to be cleared by software
- UART0~5 support data matching function
- UART0 and UART1 can generate DMA requests
- UART2~5 cannot generate DMA requests
- UART0~5 support waking up from STOP Mode:
  - The falling edge of the START bit can wake up STOP Mode
  - Provides corresponding wake-up interrupt enable bit WKIE and wake-up interrupt flag WKIF

Note: Ports of UART3 support two mapping schemes:

- Mapping 1: RXD3 / TXD3
- Mapping 2: RXD3A / TXD3A

When Mapping 1 (RXD3/TXD3) is selected, these pins are multiplexed with the system's programming/debug interface (T_CLK / T_DIO). Under this mapping, if full-duplex communication is enabled, T_CLK / T_DIO might conflict with the receive timing of UART3's RXD3, leading to communication

abnormalities. Therefore, when selecting Mapping 1, UART3 must be configured for half-duplex communication mode to avoid this hardware conflict and ensure communication stability.

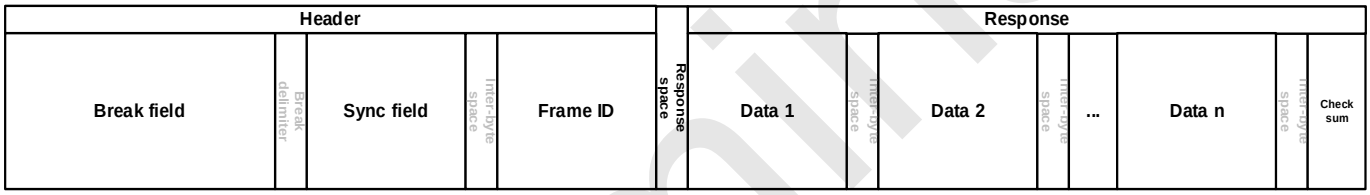
If full-duplex UART communication is required, please map the pins to Mapping 2 (RXD3A/TXD3A).

17.3 UART2-LIN

UART2 supports standard LIN communication protocol.

17.3.1 LIN Frame Structure

Under the LIN protocol, all communication information is encapsulated into frames. A frame is composed of a header (provided by the master task) and a response (provided by the slave task). The header (provided by the master task) consists of a break field, a sync (synchronization) field and a frame ID. The frame ID serves solely to define the purpose of the frame, and the slave is responsible for responding to the relevant frame ID. The response consists of a data field and a checksum field.



LIN Frame Structure Diagram

17.3.2 LIN Master Mode

By setting FUNCSEL=1 and SLVEN=0, the UART will support LIN master mode. In LIN mode, according to the LIN protocol, each byte is initiated with a dominant bit, followed by 8 data bits with no parity bit, LSB first, and ends with a recessive STOP bit.

The initialization process for LIN master mode is as follows:

① Configure the UART_BAUD register to set the baud rate
② Set FUNCSEL=1 to select the LIN function mode
③ Set SM[1:0] to 01 to configure the UART in Mode 1

A complete header consists of a break field, a sync field, and a frame ID. The UART controller can choose the 'break field' as the transmitted header. The 'sync field' and 'frame ID field' need to be written by the user through software, that is to say, to send a complete header to the bus, the software must sequentially fill in the sync data (0x55) and the frame ID data into the UART_DAT register."

17.3.3 LIN Slave Mode

By setting FUNCSEL=1 and SLVEN=1, the UART will support LIN slave mode. In LIN mode, according to the LIN protocol, each byte is initiated with a dominant bit, followed by 8 data bits with no parity bit, LSB first, and ends with a recessive STOP bit.

The initialization process for LIN slave mode is as follows:

① Configure the UART_BAUD register to set the baud rate.
② Set FUNCSEL=1 to select the LIN function mode.
③ Set SM[1:0] to 01 to configure the UART in Mode 1.
④ Set SLVEN to 1 to enable LIN slave mod.

In LIN slave mode, the slave break field detection function is enabled by setting LBDL to detect and receive 'break field'. After receiving a break, the BKIF flag will be set and an interrupt will be generated if BKIE is set to 1. To avoid bit rate deviation, users can set SLVAREN to enable automatic resynchronization feature to prevent clock errors.

17.3.3.1 Synchronization Error Detection

In automatic resynchronization mode, the controller will detect errors in the sync field. The error detection compares the current baud rate with the baud rate of the received sync field, and the following both detections are performed simultaneously.

Check 1: Based on the measurements from the first falling edge to the last falling edge of the sync field,

- If the error exceeds 15%, the header error flag SLVHEIF will be set
- If the error is between 14% and 15%, the header error flag SLVHEIF may be set (depending on data dephasing)

Check 2: Based on the measurements from each falling edge of the sync field,

- If the error exceeds 19%, the header error flag SLVHEF will be set
- If the error is between 15% and 19%, the header error flag SLVHEIF may be set (depending on data dephasing)

Note: Error detection is based on the current baud rate clock. Therefore, to ensure the accuracy of error detection, it is recommended that users reload the baud rate to its initial value through software before a new break field is received.

18 Smart Card Interface (SMCI)

18.1 Overview

The SC32L14T/14G series' built-in smart card interface controller is based on the ISO/IEC 7816-3 standard and can communicate 8-bit data serially over two lines. Software-controlled GPIO pins can be used for smart card reset and smart card insertion detection.

18.2 Clock Source

The SC32L14T/14G SMCI has only one clock source, which is derived from HCLK.

18.3 Feature

The SC32L14T/14G smart card interface features are as follows:

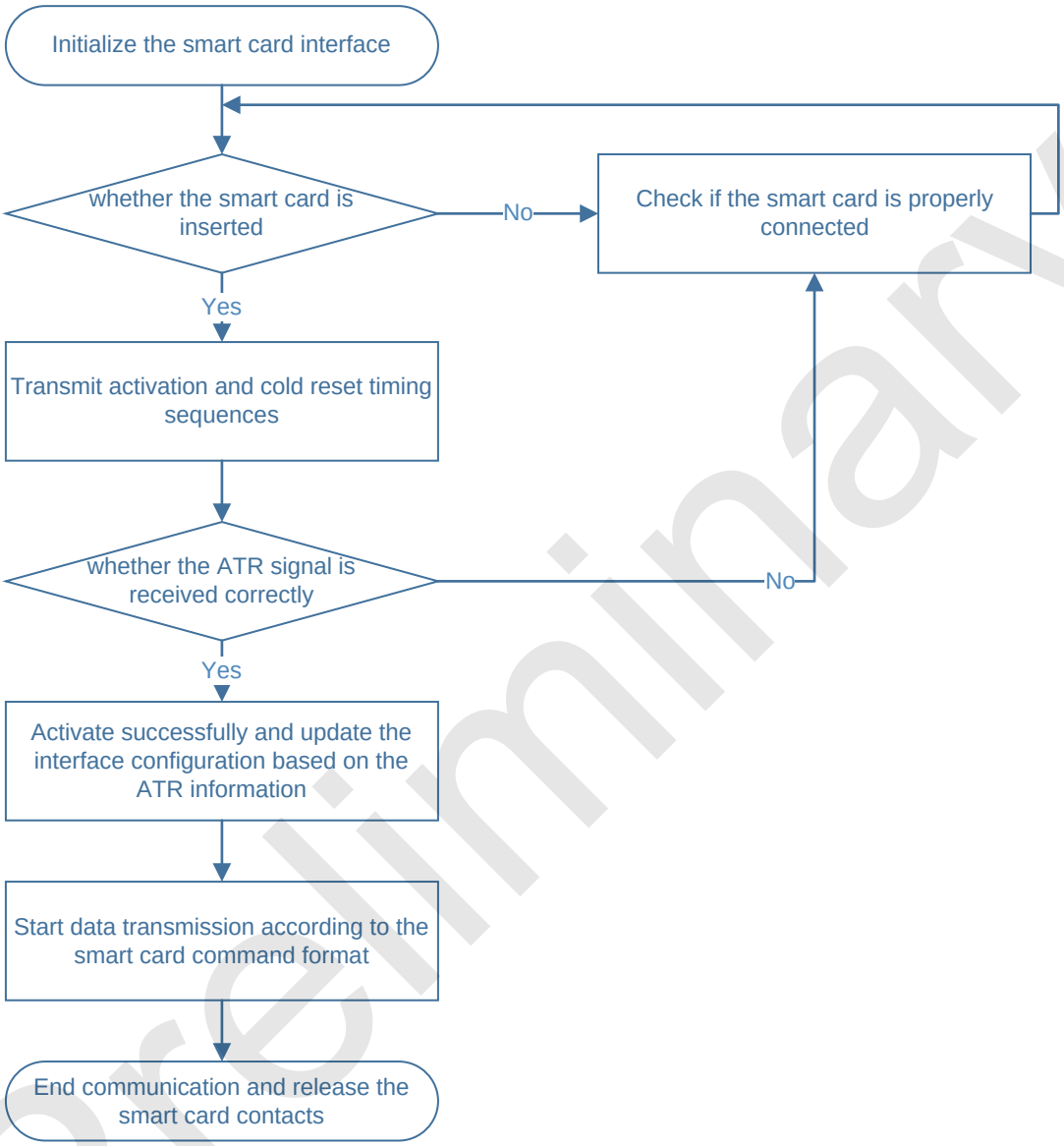
- Supports the ISO 7816-3 T = 0 asynchronous half-duplex transmission protocol standard
- Both direct convention and inverse convention are supported
- Programmable clock source frequency f_{SC}
- Flexible and adjustable Basic Time Unit (ETU)
- Configurable Extended Protection Time
- Data Frame Control:
  - Supports programmable parity mode: Even Parity or No Parity
  - Automatically generate and detect parity bit
  - Configurable stop bit length (1-2 bits)
  - Error indication signal (Error Signal) pulse width can be set
- Signal ports can be mapped to 2 sets of ports

18.4 Operating Modes

18.4.1 Smart Card Description

The smart card interface controller supports activation, cold reset, warm reset, and release sequences. A detailed description can be found in the "SC32L14T_14G_TRM”.

18.5 Basic Smart Card Interface Operation Flow



19 SPI0/1

19.1 Clock Source

The SC32L14T/14G SPI has only one clock source, which is derived from PCLK.

19.2 SPI0/1 Feature

- SPI0/1 and TWI0/1 operate independently with multiplexed register addresses and signal pins
- Supports 13-stage SPI clock pre-scaling
- Signal ports can be mapped to 4 additional sets of portsSupport receive buffer overflow interrupt and corresponding flag to promptly notify exceptions
- Support master mode or slave mode
- Both SPI0/1 can generate DMA request

20 TWI0/1

20.1 Clock Source

The SC32L14T/14G TWI has only one clock source, which is derived from PCLK.

20.2 TWI0/1 Feature

- SPI0/1 and TWI0/1 operate independently with multiplexed register addresses and signal pins
- Supports 11-stage TWI clock pre-scaling. The default TWI communication rate in master mode is the minimum prescaler (f_{PCLK}/4)
- Signal ports can be mapped to 4 sets of ports
- Support master/slave mode
- Bidirectional data transmission between master and slave
- Supports clock stretching
- Both TWI0/1 can generate DMA requests

20.3 TWI Signal Description

On the TWI bus, data is synchronously transmitted between the master and slave devices using the clock line (SCL) and the data line (SDA). Each data byte has a length of 8 bits, and one data bit is transferred with each SCL clock pulse. The data is transmitted starting from the most significant bit (MSB), and after each byte, an acknowledgment bit follows. Each bit is sampled when SCL is high. Therefore, the SDA line may change when SCL is low, but it must remain stable when SCL is high. When SCL is high, any transition on the SDA line is considered a command (START or STOP).

TWI Clock Signal Line (SCL)

The clock signal is generated by the master and is connected to all the slaves. It transmits one byte of data every 9 clock cycles. The first 8 cycles are used for data transmission, and the last one is used as the acknowledgment clock for receiver. It should be pulled up by the pull-up resistor on the SDA line when idle.

TWI Data Signal Line (SDA)

SDA is a bidirectional signal line and should be pulled up by the pull-up resistor on the SDA line when idle.

21 Hardware Watchdog WDT

21.1 Overview

The SC32L14T/14G series features a built-in hardware watchdog (WDT) with an internal 32kHz oscillator LIRC as its clock source. Users can choose to enable the watchdog reset function by setting the ENWDT control bit in the Customer Option through a programmer.

The WDT is known for its high safety, accurate timing and flexible usage. This watchdog peripheral can detect and resolve faults caused by software errors, and it will trigger a system reset when the counter reaches overflow time.

The WDT is driven by its internal low-frequency oscillator, which allows it to remain operational even if the main clock fails.

21.2 Clock Source

The SC32L14T/14G series WDT is fixed to LIRC. Once the WDT is enabled, LIRC will automatically start, and it will remain oscillating throughout the operation of the WDT and users cannot turn off LIRC while the WDT is active.

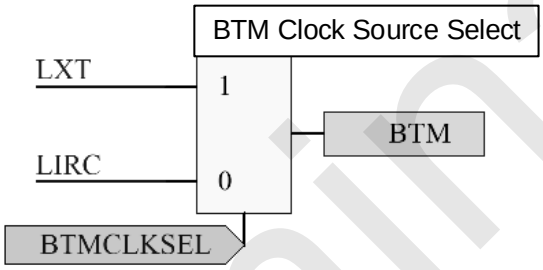
22 BTM

22.1 Overview

The SC32L14T/14G series features a Base Timer (BTM) that can generate interrupts at intervals ranging from 15.625ms to 32s. The BTM can use either 32kHz LIRC or external 32.768kHz crystal oscillator (LXT) as its clock source. The interrupts generated by the BTM can wake up the CPU from STOP mode.

22.2 Clock Source

The SC32L14T/14G series BTM can choose LXT or LIRC as its clock source.



22.3 Feature

- Can choose LXT or LIRC as its clock source
- Selectable interrupt frequency intervals from 15.625ms to 32s
- Can wake up from STOP Mode

23 Built-in CRC Module

23.1 Overview

The SC32L14T/14G series has a built-in CRC (Cyclic Redundancy Check) module that utilizes a polynomial generator to generate CRC codes from an 8-bit/16-bit/32-bit data word. In numerous applications, CRC-based techniques are commonly used to verify the integrity of data transmission or storage. According to the functional safety standards, these techniques offer a means to verify the integrity of Flash. The CRC calculation unit helps compute the software signature during runtime, and this signature is then compared with the reference signature generated at link time and stored in a designated storage unit.

23.2 Clock Source

The SC32L14T/14G CRC has only one clock source, which is derived from HCLK.

23.3 Feature

- 1 built-in hardware CRC module
- Configurable initial value, with a default of 0xFFFF_FFFF
- Supports 8-bit/16-bit/32-bit data units
- Programmable polynomial, with a default of 0x04C1_1DB7
- Only supports software-driven data computation mode
- Supports DMA: CRC_DR can serve as the DMA destination address or be accessed directly via registers
- Calculating CRC for a single byte requires 1 system clock

CRC algorithm	CRC-32/MPEG-2
Polynomial Formula	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1$
Data Width	32bit
Initial Value	0xFFFF_FFFF
Result XOR Value	0x0000_0000
Input Value Reversal	false
Output Value Reversal	false
LSB/MSB	MSB

Note: The written and read data in CRCDR cannot be the same.

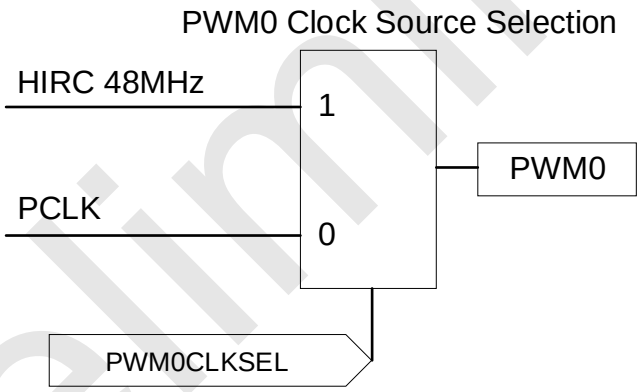
24 PWM0: 8 Channels of 16-bit Multifunctional PWM

24.1 Overview

The PWM0 of the SC32L14T/14G series is an 8-channel 16-bit shared-cycle multifunctional PWM. PWM0 has rich functionalities, including support for adjusting the cycle and duty cycle, the option to choose between center-aligned or edge-aligned output waveforms, selectable independent or complementary output modes, support for dead-time functionality, and a fault detection mechanism. The Register PWM0_CON and PWM0_STS control the state and cycle of the PWM. Each channel of PWM can be individually adjusted for enabling, output waveform, waveform inversion, and duty cycle.

24.2 Clock Source

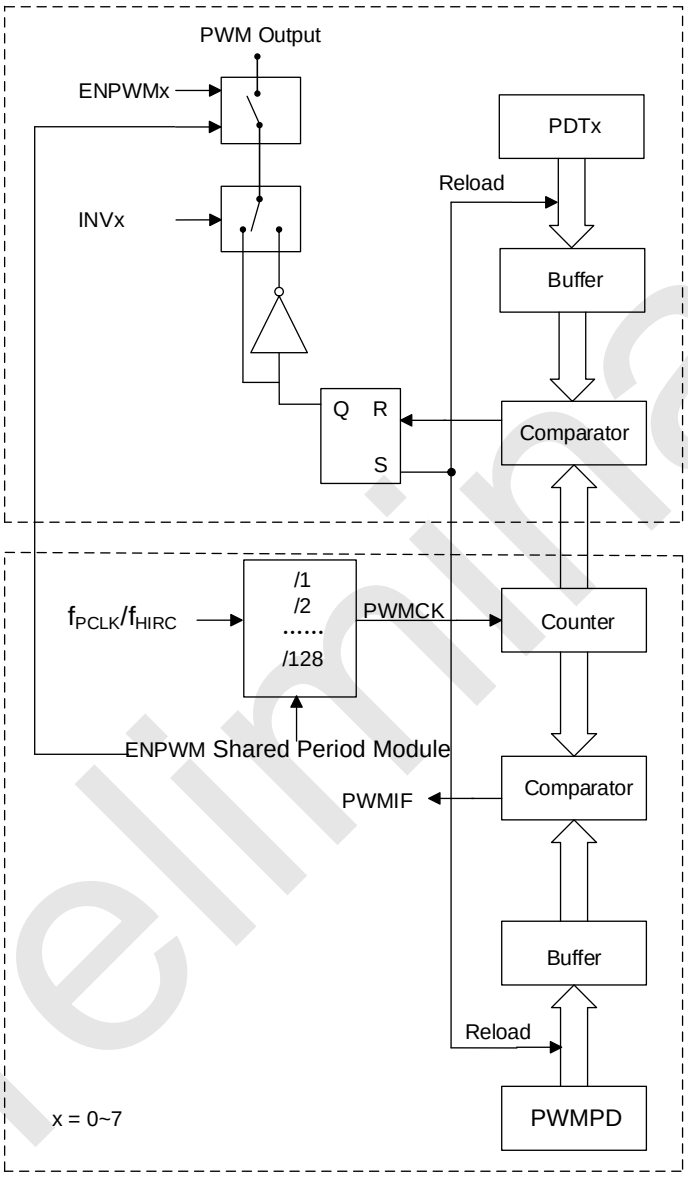
- The SC32L14T/14G PWM0 can choose 48MHz HIRC or PCLK as its clock source
- Selectable PCLK and HIRC
- PWM0 output frequency is at its maximum the frequency of HIRC



24.3 Feature

- 8 channels of 16-bit shared-period multifunctional PWM
- The output waveform can be inverted
- Waveform types: can be set as center-aligned or edge-aligned
- PWM modes: can be set as independent mode or complementary mode:
  - In independent mode, all 8 PWM channels share the same period, but the duty cycle of each PWM channel can be adjusted independently
  - In complementary mode, four pairs of complementary PWM waveforms with dead time can be generated simultaneously
- Provides one PWM overflow interrupt
- Supports fault detection
- Has independent interrupt request flags

24.4 PWM0 Structure Diagram



PWM0 Structure Diagram

24.5 PWM0 General Configuration

24.5.1 Output Mode

- In independent mode, all 8 PWM channels share the same period, but the duty cycle of each PWM channel can be adjusted independently
- In complementary mode, four pairs of complementary PWM waveforms with dead time can be generated simultaneously

24.5.2 Alignment Type

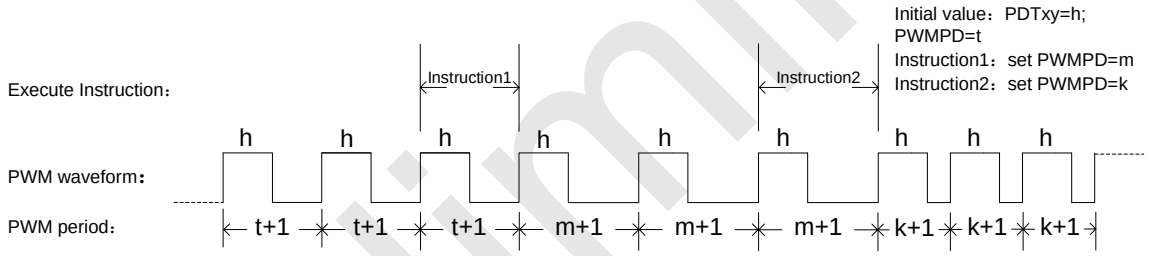
- Edge-aligned
- Center-aligned

24.5.3 Duty Cycle Change Characteristics

When generating the PWM0n output waveform, if it is necessary to change the duty cycle, it can be achieved by modifying the high-level setting register (PDT0x). However, it is important to note that changing the value of PDT0x will not immediately alter the duty cycle. Instead, the change takes place when the PWM counter counts to 0 or counts up to a value matching the setting in the period setting item PWMPD[15:0] +1.

24.5.4 Period Change Characteristics

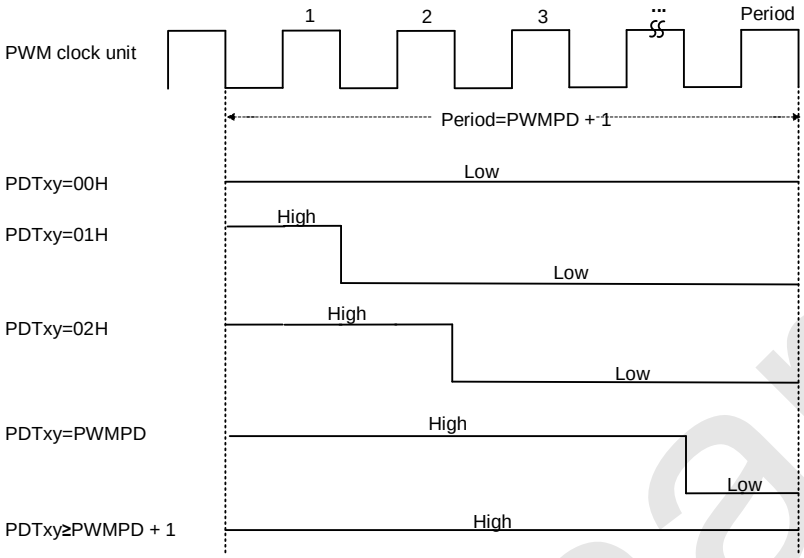
When generating PWM output waveforms, if it is necessary to change the period, it can be achieved by modifying the period setting register PWMPD. Similar to the duty cycle, changing the value of PWMPD will not immediately alter the period. The change takes place when the PWM counter counts to 0 or counts up to a value matching the setting in the period setting item PWMPD[15:0] +1.



Period variation characteristics diagram

24.5.5 Relationship Between Period and Duty Cycle

The assumption for this result is that the initial value of PWM output inversion control (INVx, x=0~7) is 0. If the opposite result is desired, INVx should be set to 1. The relationship between period and duty cycle is as follows：



Period and Duty Cycle Relationship Diagram

25 32-Channel High-Sensitivity Touch Circuit (TK)

- High-sensitivity mode
- Suitable for touch applications with high sensitivity requirements, such as proximity sensing and touch keys
- Can pass 10V dynamic CS test
- Channels can be scanned in parallel
- 103 Capacitor must be connected between the CMOD pin and ground
- Support self-capacitance mode and mutual-capacitance mode
- Supports low-power mode
- Support fast wake-up from STOP Mode
- Comprehensive development support: Highly flexible touch software library, intelligent debugging software

26 Real-Time Clock (RTC)

26.1 Overview

The SC32L14T/14G series integrates a real-time clock (RTC). The RTC is an independent BCD timer /counter that provides a calendar clock with a programmable alarm function. The RTC can operate in normal mode, low-power mode, or reset state. In low-power mode, the RTC can also serve as a wake-up unit.

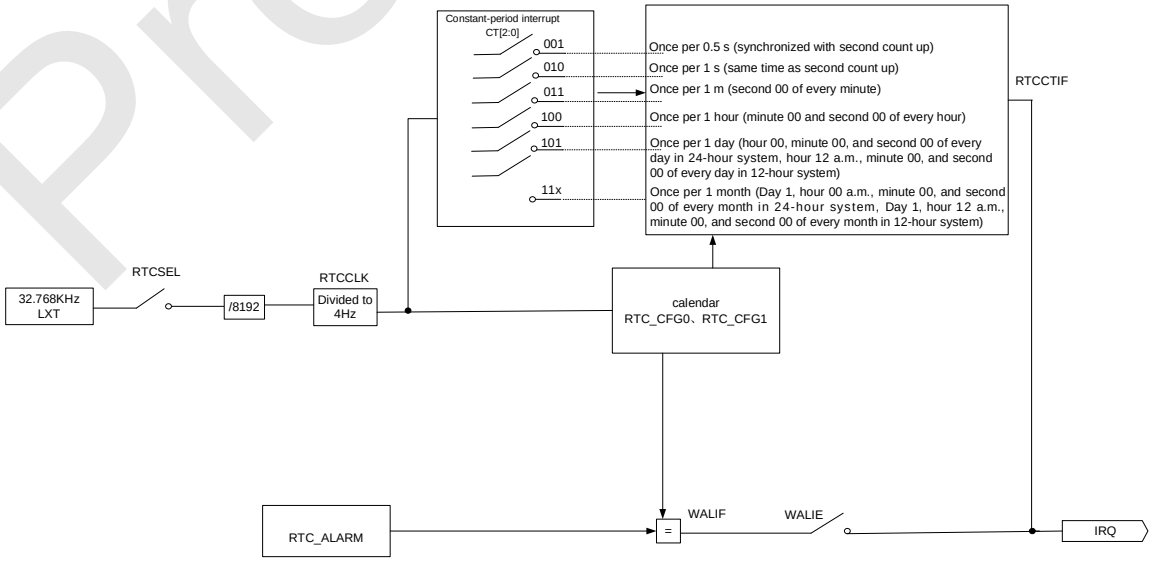
26.2 Clock Source

The SC32L14T/14G RTC has only one clock source, which is derived from LXT.

26.3 Feature

- Clock source is LXT
- Can run in low power mode and support wake-up from STOP Mode
- Perpetual Calendar Function
  - Support BCD format time/date registers
  - Automatically correction for 28, 29 (leap year), 30, and 31 days of the month
  - Accuracy follows external 32.768K crystal oscillator (LXT)
- Interrupt system
  - Alarm interrupt function
  - Constant-period interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month, 1 year)
  - Supports waking up STOP mode through interrupt events
- Time mode configuration
  - Supports the 12- or 24-hour system
- Secure Read/Write Mechanism:
  - Independent half-second flag: users can perform register read and write operations when the half-second flag is set, avoiding timing conflicts caused by the carry process
- Register synchronization design: after writing time data, the read operation immediately returns the written value (buffering mechanism), but the actual effect requires a 250ms synchronization period (registers are not updated during this period)

26.4 Block Diagram



27 Low-Power Counter (LPC)

27.1 Overview

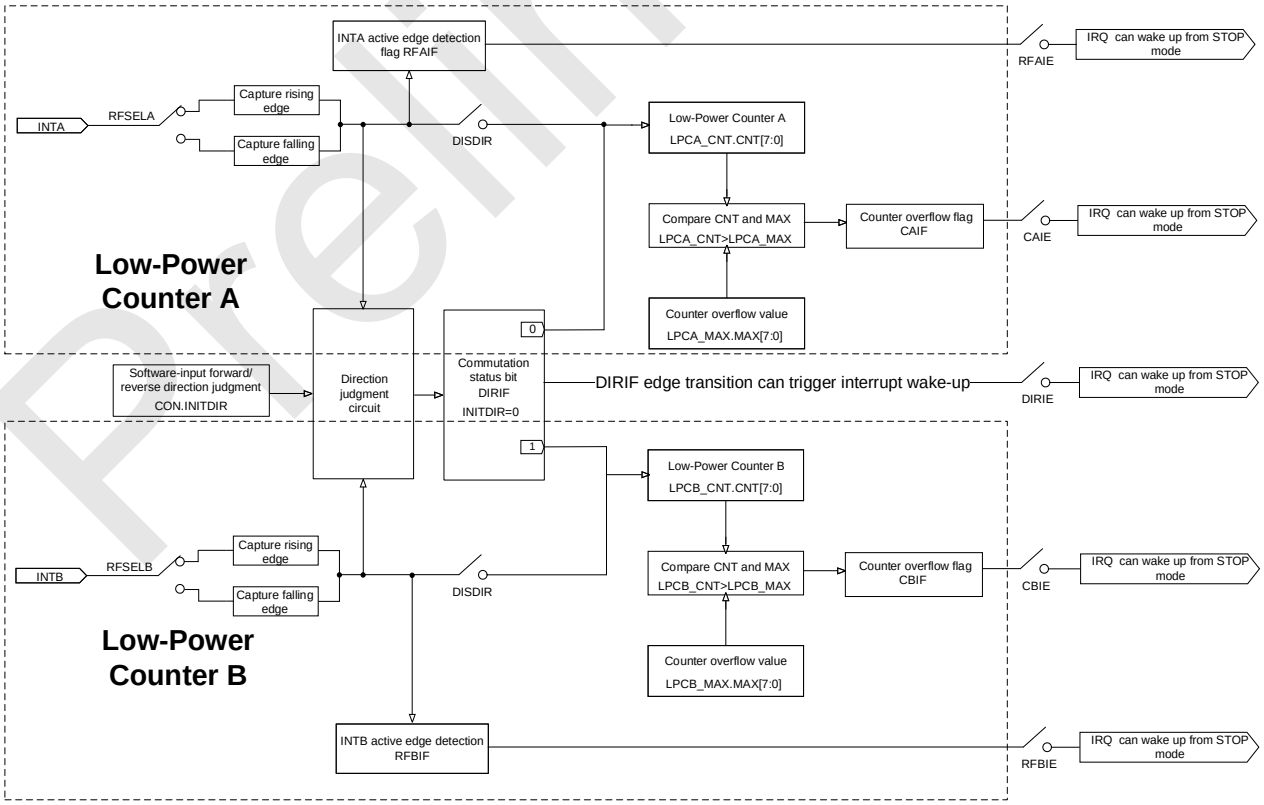
The SC32L14T 14G integrates a low-power counter (LPC) that can be connected to devices such as linear or incremental encoders to obtain information such as count and direction. The LPC supports counting in STOP mode, reducing the MCU wake-up frequency and overall power consumption.

The LPC provides two independent edge detection channels, INTA and INTB. Each channel has an independent counter with independent settings for rising and falling edge validity and count overflow values. Hardware can determine the direction of the two input signals. All interrupt events (including two edge detection interrupts, two counter overflow interrupts, and one direction jump interrupt) can wake up STOP mode.

27.2 Feature

- Can be connected to devices such as linear or incremental encoders to obtain counting, direction and other information
- Can count in STOP mode, reducing MCU wake-up frequency and overall power consumption
- Two external signal input ports, INTA and INTB, are provided, which can independently detect the rising and falling edges of the input signals and count them independently
  - Edge detection can trigger an interrupt
  - A count overflow can trigger an interrupt
- The direction information of the input signal can be judged in hardware
  - A direction change can trigger an interrupt
- LPC interrupts can wake up STOP mode

27.3 LPC Block Diagram



28 16-bit Timers (Timer0~Timer7)

28.1 Clock Source

- In timer mode/PWM output mode, the TIM clock source is derived from PCLK
- In counter mode, the Tn pin serves as the counting source input

28.2 Feature

- Supports 8-stage TIM clock pre-scaling
- 8 independent 16-bit auto-reload counters: Timer0 to Timer7
- 16-bit incremental, decremental, and increment/decrement auto-reload counters
- Support rising/falling edge capture, enabling PWM duty and period capture
- Each TIM provides two PWM (TPWMA / TPWMB) outputs with a shared period and adjustable duty cycles
- Overflow and capture events of TIM1/2/6 can generate DMA requests
- Each Tn of TIM0~7 can be mapped to another sets of IO pins

28.3 Counting method

28.3.1 Counting Method in Timer Mode

- Upward Counting: Counts from the set value upwards to overflow at 0xFFFF
- Downward Counting: Counts from 0xFFFF downwards to the set value

28.3.2 Counting Method in PWM Mode

Only upward counting mode is available in PWM output mode: The counter starts from 0 and counts up until PDT, then PWM output waveform will switch between the high and low levels. The counting will then continue up to RLD, causing an overflow and the counter reset to 0.

The formula of TPWM is shown as follows:

$$T_{PWM} = \frac{RLD[15:0] + 1}{PCLK}$$

The formula of duty is shown as follows:

$$duty = \frac{PDT[15:0]}{RLD[15:0] + 1}$$

28.4 Timer Signal Port

- Tn/TnCAP, n=0~7
  - Tn Clock input/output

  - Both TnCAP rising and falling edges can be captured
  - Note: Tn and TnCAP are multiplexed functions and cannot be used simultaneously
- TnEX, n=0~7
  - In reload mode, the external event input (falling edge) on the TnEX pin is used for reload enable/disable control
  - In capture mode, when FSEL = 1, it serves as a falling edge capture signal input. Detection of a falling edge on the TnEX pin generates a capture, sets EXIF, and captures the value of the TnCNT register into the FCAP register
- TnPWM, n=0~7
  - TIM0~7 can provide PWM with independently adjustable duty cycle through the Tn port: TnPWMA
  - TIM0~7 can provide PWM with independently adjustable duty cycle through the TnEX port: TnPWMB
  - TnPWMA and TnPWMB share a common period, with their clock source following that of the TIM

Note: TIM's PWM capture function and PWM output function cannot be enabled simultaneously

28.5 Interrupts and Corresponding Flags for TIM

- Overflow/underflow of the counter share the interrupt flag TIF
- Capture status flags:
  - EXIF: Flag indicating detection of a falling edge on the external event input
  - EXIR: Flag indicating detection of a rising edge on the external event input
- Interrupt and priority configuration control bits are merged into the NVIC module

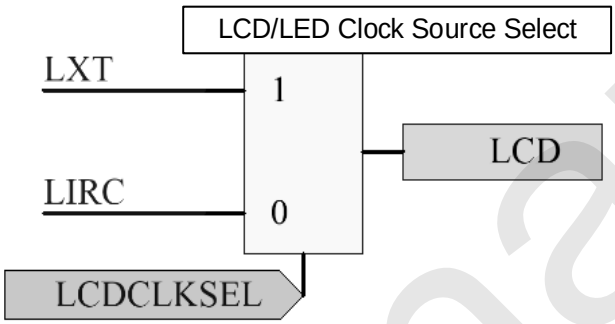
28.6 Timer Operating Mode

- Mode 0: 16-bit capture mode, capable of PWM edge capture on both rising and falling edges
- Mode 1: 16-bit auto-reload timer/counter mode
- Mode 3: Programmable clock output mode
- Mode 4: PWM output mode

29 LCD Driver

29.1 Clock Source

- LXT and LIRC are optional
- SC32L14T/14G LCD can choose LXT or LIRC as its clock source through LCDCLKSEL bit



29.2 Built-in 8 COM x 51 SEG LCD Driver

- Support display in STOP mode
- Provides two different ways of LCD driver:
  - Resistor LCD driver: Resistor LCD driver supports fast charge mode, LCD voltage output port voltage divider resistor options: 11KΩ, 100KΩ, 300KΩ, 800KΩ
  - Capacitor LCD driver: Capacitor LCD driver is in capacitive bias mode. In this mode, the total power consumption of the LCD circuit can be as low as: 2~3μA @STOP mode
- Type A / Type B waveform selectable
- 8 X 51、6 X 53、5 X 54、4 X 55
- LCD display driver bias voltage:
  - 1/4 bias voltage
  - 1/3 bias voltage
- Three selectable frame rates:
  - Type A mode 32/64/128Hz
  - Type B mode 64/128/256Hz

29.2.1 Resistor LCD driver

When DDR_CON.LCDSEL = 0, the LCD driver is a resistor LCD driver.

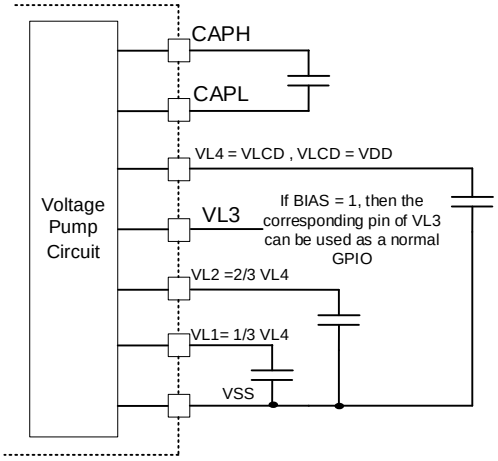
The voltage of the resistor LCD driver can be adjusted via DDR_CFG.VLCD[3:0]:

$$V_{LCD} = V_{DD} * \frac{17 + VLCD[3:0]}{32}$$

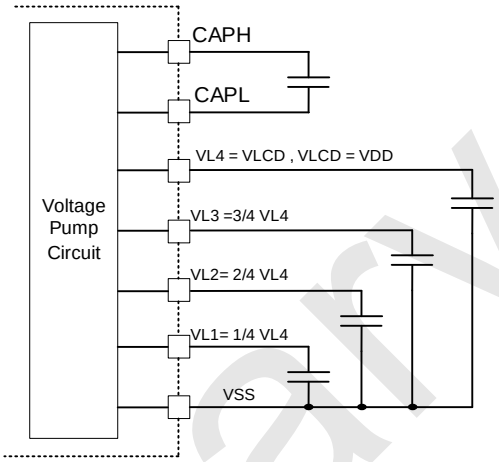
29.2.2 Capacitor LCD driver

When DDR_CON.LCDSEL = 1, the LCD driver is a capacitor LCD driver.

When selecting capacitor LCD driver, you must also write 1 to DDR_CON.PUMPON to enable the pump circuit. The LCD drive voltage (V_{LCD}) of Capacitor bias voltage mode is V_{DD}.



1/3 Bias



1/4 Bias

Note:

1.When selecting the capacitor LCD driver, connect capacitors with a capacitance of 0.47μF ±30% and minimal leakage current between CAPH and CAPL, as well as between the LCD driver power pins VLn (n=1~4) and Ground.

2.If DDR_CON.BIAS = 1, set the bias voltage to 1/ 3, then the corresponding pin of VL3 can be used as a normal GPIO

30 Direct Memory Access (DMA)

30.1 Overview

The DMA controller is designed for high-speed data transfer, allowing the movement of data from one address to another without the need for CPU intervention. Leveraging DMA for data transfer can reduce the workload on the CPU, enabling the saved CPU resources to be utilized for other applications. The DMA controller comprises 2 channels, each directly connected to dedicated hardware DMA requests. Additionally, each channel supports software triggering. The DMA controller features support for 2-level channel priority, facilitating the management of priority between DMA requests to ensure that only one DMA channel operates at any given time. It also supports both single and batch transfers, with the request source being either a software request or an interface request. Data transfer between memories is accomplished using software requests.

Note: For a bidirectional data transfer application, two DMA channels are required to handle sending and receiving operations.

30.2 Clock Source

The clock source of DMA is derived from HCLK, and the external peripheral clock of DMA is enabled through AHB_CFG.DMAEN.

30.3 Feature

- Support 2 independent configurable channels
- Support 2 priority levels for requests
- Support 8-bit, 16-bit, 32-bit data transfers
- Support automatic increment or fixed source and destination addresses, with data widths of byte, half-word, and word
- Support single and burst transfer modes
- Support memory-to- memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers

30.4 Function Description

30.4.1 Transmission

No transmit limitation between peripheral and memory for DMA：

Memory-to-Memory	Memory-to-Peripheral	Peripheral-to-Memory	Peripheral-to-Peripheral
No limitation	No limitation	No limitation	No limitation

30.4.2 DMA Access Restriction

Users are not allowed to perform write operations on Flash or access the core through DMA. Violating these restrictions may lead to unpredictable exceptions.

30.4.3 Channel Priority

There are 2 priority levels can be configured through PL[1:0] registers:

- 0: Low
- 1: High

30.4.4 Single Transmission and Burst Transmission

The DMA controller supports single and burst data transfer types, and the request source can be a software request or an interface request while data transfer between memory is done by software requests. Single transfer means that the software or interface is ready to transfer one data (each data requires one request), while burst transfer means that the software or interface will transfer multiple data (multiple data requiring only one request).

The modes of single and burst transfer can be set through TPTYPE register (DMAn_CFG[15]).

In single transfer mode, each transfer of data requires one request. As each data is transferred, the values in the register DMAn_CNT[31:0](n=0~3) decrease by 1, the transfer of data is completed when the count in DMAn_CNT[31:0] becomes 0. In this mode, BURSIZE (DMAn_CFG[14:12]) is not used to control the size of the transferred data and its value is fixed at 1.

In burst transfer mode, DMA transfer DMAn_CNT[31:0] data with only one request. After transferring BURSIZE (DMAn_CFG[14:12]) data, the value in DMAn_CNT[31:0] is decreased by BURSIZE. The transfer of data is completed when the count in DMAn_CNT[31:0] becomes 0.

30.4.5 Loop Mode

The loop mode can be used to handle circular buffers and continuous data streams (such as ADC scan mode). During the loop mode transfer, the number of data to be transferred will automatically reload to the initial value set in the channel configuration phase and continue to respond to DMA requests. To stop loop transfer, the software needs to stop the generation of DMA requests by the peripheral before disabling the DMA channel (for example, exiting ADC scan mode). The software must explicitly set the DMACNT value before starting/enabling the transfer and after stopping the loop transfer.

The SC32L14T/14G series DMA controller supports normal mode and loop mode, which users can flexibly select based on actual requirements:

- When CIRC=0 (DMA channel is in non-loop mode), it will no longer accept any DMA requests after reaching the set number of data to be transferred
- When CIRC=1 (DMA channel is in loop mode), after the transfer is complete, the DMACNT of the channel will automatically reload the previously set value and wait for the next loop

Users can flexibly choose according to their actual needs.

31 SysTick

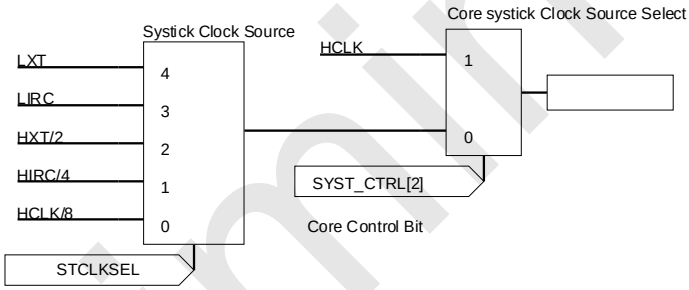
SysTick is a simple, 24-bit, writable-clear, decrementing automatic reload counter with a flexible control mechanism. This counter can be used as a tick timer for a Real-Time Operating System (RTOS) or as a simple counter.

31.1 Clock Source

SysTick (Cortex®-M0+ Core System Timer) has internal clock source and external clock source：

- Internal clock source: CPU Clock
- 5 external clock sources

SysTick clock source diagram is as follow:



31.2 SysTick Calibration Register Default Value

The calibration value for the SysTick Calibration Register is set as follows:

- If the default clock after power-on is f_{HCLK}/n (MHz), where n is the default power-on divider, and the default clock source is HIRC
- Then, setting the initial SysTick calibration value to 1000 * (f_{HCLK}/n) will generate a 1ms time reference

32 Electrical Characteristics

Unless otherwise specified, the electrical data in this section are based on the working conditions listed in the “Recommended Operating Conditions” subsection.

32.1 Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	Conditions
V_{DD}	Operating voltage	1.8	5.5	V	f_{HCLK}=48MHz Clock source is HIRC
T_A	Ambient temperature	-40	105	℃	

32.2 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC supply voltage	-0.3	6	V
V_{PIN}	Input/output voltage of any pin	-0.3	V_{DD}+0.3	V
T_A	Ambient temperature	-40	105	℃
T_{STG}	Storage temperature	-55	125	℃
I_{VDD}	Current value flowing through VDD	-	200	mA
I_{VSS}	Current value flowing through VSS	-	200	mA

32.3 Flash ROM Parameters

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
N_{END}	Endurance Erase/write cycles	100,000	-	-	Cycles	V_{DD}=5V T_A=25 ℃
T_{DR}	Data retention time	100	-	-	Years	
$T_{S\text{-}Erase}$	Single sector erase time	-	2.5	-	ms	
T_{Erase}	Full erase time	30	-	40	ms	
T_{Write}	Single byte write time	-	150	-	μs	

32.4 Power Consumption

32.4.1 V_{DD} = 5V, T_A = +25℃, boot from APROM unless otherwise specified

Symbol	Parameter	Min	Typical	Max	Unit	Conditions	
						System clock	Clock source
I_{OP1}	Operating Mode current	-	6.1	-	mA	f_{HCLK}=48MHz	Clock Source is HIRC/1 (Configuration Conditions Below: HIRC_NDIV=1 SYSCLKSEL[1:0]=10 SYSCLKSW=1）
		-	4.3	-	mA	f_{HCLK}=24MHz	Clock Source is HIRC/2 (Power-On Default Clock Source)
		-	2.8	-	mA	f_{HCLK} =12MHz	
		-	2.2	-	mA	f_{HCLK} =6MHz	
		-	1.5	-	mA	f_{HCLK} =3MHz	
I_{OP2}	Operating Mode current	-	0.2	-	mA	f_{HCLK} =32.768kHz	Clock Source is LXT
I_{OP_RTC}	Operating Mode total current with RTC enabled	-	0.2	-	mA		
$I_{OP\_LCD\_R}$	Operating Mode total current with resistor LCD driver enabled	-	0.2	-	mA		
$I_{OP\_LCD\_C}$	Operating Mode total current with capacitor LCD driver enabled	-	0.2	-	mA		
I_{IDL1}	Operating Mode current	-	1.4	-	mA	f_{HCLK}=24MHz	Clock Source is HIRC/2 (Power-On Default Clock Source)
		-	1.1	-	mA	f_{HCLK} =12MHz	
		-	1.0	-	mA	f_{HCLK} =6MHz	
		-	0.9	-	mA	f_{HCLK} =3MHz	
I_{PD1}	STOP Mode current	-	0.7	-	μA	\	\
I_{PD_RTC}	STOP Mode total current with RTC enabled	-	1.3	-	μA	f_{HCLK} =32.768kHz	Clock Source is LXT
$I_{OP\_LCD\_R}$	STOP Mode total current with resistor LCD driver enabled	-	8	-	μA		
$I_{OP\_LCD\_C}$	STOP Mode total current with capacitor LCD driver enabled	-	1.6	-	μA		

32.4.2 V_{DD} = 3.3V，T_A = +25℃, boot from APROM unless otherwise specified.

Symbol	Parameter	Min	Typical	Max	Unit	Conditions	
						System clock	Clock source
I_{OP3}	Operating Mode current	-	6.1	-	mA	f_{HCLK}=48MHz	Clock Source is HIRC/1 (Configuration Conditions Below: HIRC_NDIV=1 SYSCLKSEL[1:0]=1 0 SYSCLKSW=1）
		-	4.3	-	mA	f_{HCLK}=24MHz	Clock Source is HIRC/2 (Power-On Default Clock Source)
		-	2.8	-	mA	f_{HCLK} =12MHz	
		-	2.2	-	mA	f_{HCLK} =6MHz	
		-	1.5	-	mA	f_{HCLK} =3MHz	
I_{OP4}	Operating Mode current	-	0.2	-	mA	f_{HCLK} =32.768kHz	Clock Source is LXT
I_{OP_RTC}	Operating Mode total current with RTC enabled	-	0.2	-	mA		
$I_{OP\_LCD\_R}$	Operating Mode total current with resistor LCD driver enabled	-	0.2	-	mA		
$I_{OP\_LCD\_C}$	Operation Mode total current with capacitor LCD driver enabled	-	0.2	-	mA		
I_{IDL2}	IDLE Mode current	-	1.3	-	mA	f_{HCLK}=24MHz	Clock Source is HIRC/2 (Power-On Default Clock Source)
		-	1.1	-	mA	f_{HCLK} =12MHz	
		-	0.9	-	mA	f_{HCLK} =6MHz	
		-	0.8	-	mA	f_{HCLK} =3MHz	
I_{PD2}	STOP Mode current	-	0.6	-	μA	\	\
I_{PD_RTC}	STOP Mode total current with RTC enabled	-	1.2	-	μA	f_{HCLK} =32.768kHz	Clock Source is LXT
$I_{OP\_LCD\_R}$	STOP Mode total current with resistor LCD driver enabled	-	5.5	-	μA		
$I_{OP\_LCD\_C}$	STOP Mode total current with capacitor LCD driver enabled	-	1.5	-	μA		

32.5 GPIO Parameter

32.5.1 V_{DD} = 5V, T_A = +25℃, unless otherwise specified

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{IH1}	Input high voltage	0.7V_{DD}	-	V_{DD}+0.3	V	
V_{IL1}	Input low voltage	-0.3	-	0.3V_{DD}	V	
V_{IH2}	Schmitt Trigger Input Port Note 1 Input high voltage	0.8V_{DD}	-	V_{DD}	V	
V_{IL2}	Schmitt Trigger Input Port Note 1 Input low voltage	-0.2	-	0.2V_{DD}	V	
I_{OL}	Output low current	-	25	-	mA	V_{Pin}=0.4V
I_{OL2}	Output low current	-	50	-	mA	V_{Pin}=0.8V
I_{OH1}	Output high current	-	12	-	mA	V_{Pin}=4.3V
I_{OH2}	Output high current	-	6	-	mA	V_{Pin}=4.7V
I_{lkg1}	Input leakage current	-1	-	1	μA	IO is in high-impedance input mode V_{IN}=V_{DD} 或 V_{SS}
R_{PH1}	Pull-up resistance	15	30	45	kΩ	V_{IN}=V_{SS}

Note 1: Schmitt Trigger input ports include: NRST, T_CLK / T_DIO, UART RX signal port, SPI / TWI signal input ports, INT0~INT15, PWM Fault Detection port (FLT), Timer clock input ports (Tn), and Timer capture ports (TnEX).

32.5.2 V_{DD} = 3.3V, T_A = +25℃, unless otherwise specified

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{IH3}	Input high voltage	0.7V_{DD}	-	V_{DD}+0.3	V	
V_{IL3}	Input low voltage	-0.3	-	0.3V_{DD}	V	
V_{IH4}	Schmitt Trigger Input Port Note 1 Input high voltage	0.8V_{DD}	-	V_{DD}	V	
V_{IL4}	Schmitt Trigger Input Port Note 1 Input low voltage	-0.2	-	0.2V_{DD}	V	
I_{OL3}	Output low current	-	20	-	mA	V_{Pin}=0.4V
I_{OL4}	Output low current	-	35	-	mA	V_{Pin}=0.8V
I_{OH3}	Output high current	-	3.5	-	mA	V_{Pin}=3.0V
I_{lkg2}	Output high current	-1	-	1	μA	IO is in high-impedance input mode V_{IN}=V_{DD} 或 V_{SS}

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
R_{PH2}	Input leakage current	25	50	75	kΩ	V_{IN}=V_{SS}

Note 1: Schmitt Trigger input ports include: NRST, T_CLK / T_DIO, UART RX signal port, SPI / TWI signal input ports, INT0~INT15, PWM Fault Detection port (FLT), Timer clock input ports (Tn), and Timer capture ports (TnEX).

32.6 AC Electrical Characteristics

(VDD = 2.0V ~ 5.5V,TA = 25℃,unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
T_{LXT}	External 32kHz oscillator start-up time	-	1	-	s	External 32kHz crystal oscillator
T_{POR}	Power On Reset time	-	15	-	ms	
T_{PDW}	Power Down Mode wake-up time	-	35	-	μs	
T_{Reset}	Reset pulse width	18	-	-	μs	low-level active
T_{LVR}	LVR debounce time	-	30	-	μs	
f_{HIRC}	HIRC oscillator stability	-1	-	+1	%	V_{DD}=1.8~5.5V T_A=-40~85 ℃
		-1.5	-	+1.5	%	V_{DD}=1.8~5.5V T_A=-40~105 ℃
f_{LIRC}	LIRC oscillator stability	-4	-	4	%	V_{DD}=1.8~5.5V T_A=25 ℃

32.7 TK Characteristics

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
I_{TK}	High sensitivity Touch key working current	-	0.9	1.3	mA	f_{HCLK}=48MHz
		-	0.8	1.2	mA	f_{HCLK}=48MHz

32.8 BTM Characteristics

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
I_{BTM}	Base Timer working current	-	1.1	3	μA	BTMCLKSEL=0 BTM Clock source is LIRC V_{DD}=5V
		-	1.0	3	μA	BTMCLKSEL=0

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
						BTM Clock source is LIRC V_{DD}=3.3V

32.9 WDT Characteristics

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
I_{WDT}	WDT working current	-	1.1	3	μA	V_{DD}=5V
		-	1.0	3	μA	V_{DD}=3.3V

32.10 ADC Characteristics

(T_A = 25℃,unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{AD1}	Supply Voltage 1	2.7	5.0	5.5	V	Vref = 2.048V
V_{AD2}	Supply Voltage 2	2.0	5.0	5.5	V	Vref = 1.024V or Vref = V_{DD}
V_{AD3}	Supply Voltage 3	2.7	5.0	5.5	V	Vref = 2.4V
V_{REF1}	Internal reference 2.048V	2.033	2.048	2.063	V	V_{DD} = 2.7~5.5V
V_{REF2}	Internal reference 1.024V	1.004	1.024	1.044	V	V_{DD} = 2.0~5.5V
V_{REF3}	Internal reference 2.4V	2.37	2.40	2.45	V	V_{DD} = 2.7~5.5V
N_R	Precision	-	14	-	bit	GND≤V_{AIN}≤V_{DD}
V_{AIN}	ADC Input voltage	GND	-	V_{DD}	V	
R_{AIN}	ADC Input resistance	1	-		MΩ	V_{IN}=5V
I_{lkg_ADC}	ADC input leakage current	-1	-	1	μA	V_{IN}=V_{AINx}
I_{ADC1}	ADC conversion current 1	-	-	2	mA	ADC Module on V_{DD}=5V
I_{ADC2}	ADC conversion current 2	-	-	1.8	mA	ADC Module on V_{DD}=3.3V
DNL	Differential nonlinear error	-	-	±9	LSB	V_{DD}=5V V_{REF}=5V
INL	Integral nonlinear error	-	-	±9	LSB	
E_Z	Offset error	-	-	±12	LSB	
E_F	Full scale error	-	-	±12	LSB	
E_{AD}	Total absolute error	-	-	±12	LSB	
T_{ADC1}	ADC sampling + conversion time 1	-	1.1	1.4	μs	LOWSP[2:0] = 100 f_{HCLK} =24MHz，

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
						Clock source is HIRC
T_{ADC2}	ADC sampling + conversion time 2	-	1.2	1.6	μs	LOWSP[2:0] = 101 f_{HCLK} =24MHz， Clock source is HIRC
T_{ADC3}	ADC sampling + conversion time 3	-	1.6	2.1	μs	LOWSP[2:0] = 110 f_{HCLK} =24MHz， Clock source is HIRC
T_{ADC4}	ADC sampling + conversion time 4	-	2.3	3.0	μs	LOWSP[2:0] = 111 f_{HCLK} =24MHz， Clock source is HIRC

32.11 CMP Electrical Characteristics

(V_{DD} =5V,T_A = 25℃, unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
V_{CM}	Input voltage range	0	-	V_{DD}	V	
V_{OS}	Offset voltage	-	10	30	mV	
V_{HYS}	comparator voltage hysteresis	-	40	-	mV	
I_{CMP}	Comparator switching current	-	-	100	μA	V_{DD}=5V
T_{CMP}	Response time	-	-	2	μs	

32.12 OP Electrical Characteristic

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
I_{OP}	OP working current	-	1	1.3	mA	V_{DD}=5V
V_{OP}	OP working voltage	2.8	-	5.5	V	
V_{OPO}	OP output voltage	V_{SS}+0.2	-	V_{DD}-0.2	V	
V_{CMI}	Common mode input voltage	0	-	V_{DD}	V	
V_{OFFSET}	Offset voltage	-1	-	1	mV	
I_{LOAD}	Load current	-	-	600	μA	
R_{LOAD}	Load resistance	8	-	-	kΩ	
C_{LOAD}	Load capacitance	-	-	30	pF	
CMRR	Common mode rejection ratio	-	90	-	dB	
PSRR	Power supply rejection ratio	-	75	-	dB	
GBW	Gain-bandwidth	-	20	-	MHz	

Slew rate	Slew rate	-	13	-	V/us	
PM	Phase margin	-	60	-	°	CL = 50pF
G_{PGA}	PGA non-inverting gain	-5	-	5	%	Non-inverting gain = 8
		-5	-	5	%	Non-inverting gain = 16
		-5	-	5	%	Non-inverting gain = 32
		-5	-	5	%	Non-inverting gain = 64
	PGA inverting gain	-5	-	5	%	Inverting gain = 7
		-5	-	5	%	Inverting gain = 15
		-5	-	5	%	Inverting gain = 31
		-5	-	5	%	Inverting gain = 63
R_{PGA}	PGA non-inverting R2/R1 internal resistance value	-	70/10	-	kΩ/ kΩ	Non-inverting gain = 8
		-	150/10	-	kΩ/ kΩ	Non-inverting gain = 16
		-	310/10	-	kΩ/ kΩ	Non-inverting gain = 32
		-	630/10	-	kΩ/ kΩ	Non-inverting gain = 64
	PGA inverting R2/R1 internal resistance value	-	70/10	-	kΩ/ kΩ	Inverting gain = 7
		-	150/10	-	kΩ/ kΩ	Inverting gain = 15
		-	310/10	-	kΩ/ kΩ	Inverting gain = 31
		-	630/10	-	kΩ/ kΩ	Inverting gain = 63
RΔ	R1/R2 resistance variation	-20	-	+20	%	

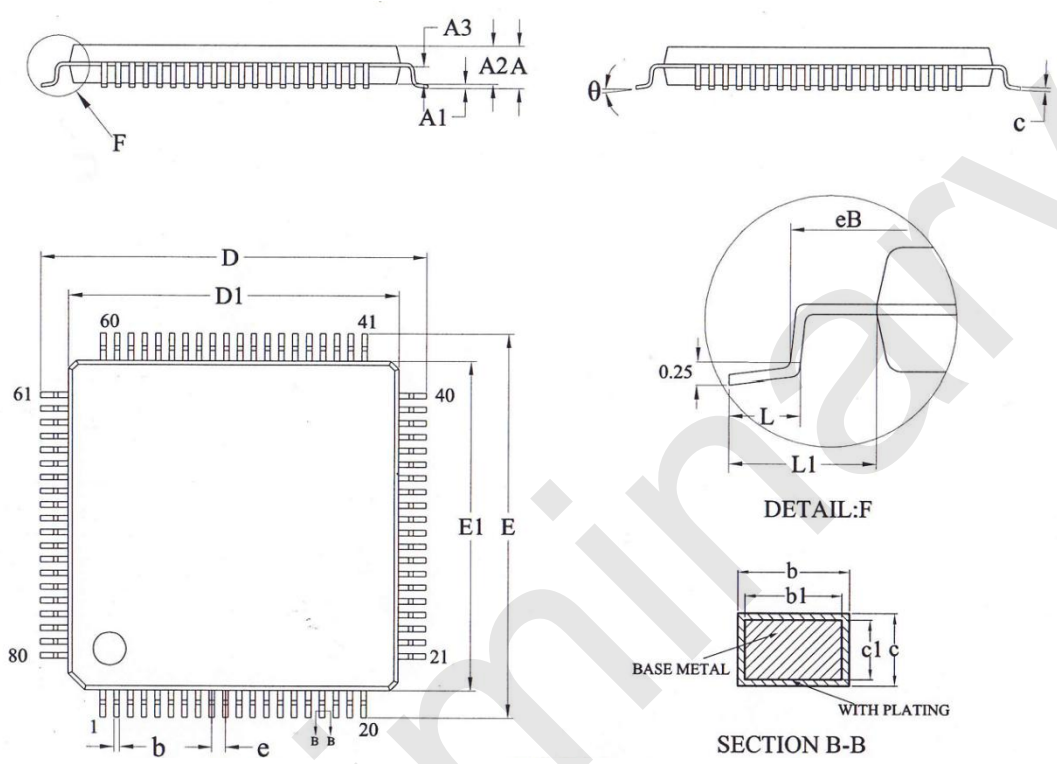
32.13 LPD Electrical Characteristics

Symbol	Grade	Parameter	Condition	Min	Typical	Max	Uint
V_{LPD0}	1.85V	LPD threshold 0	Falling edge	-	1.84	-	V
			Rising edge	-	1.94	-	
V_{LPD1}	2.05V	LPD threshold 1	Falling edge	-	2.04	-	
			Rising edge	-	2.14	-	
V_{LPD2}	2.25V	LPD threshold 2	Falling edge	-	2.24	-	
			Rising edge	-	2.34	-	
V_{LPD3}	2.45V	LPD threshold 3	Falling edge	-	2.44	-	

Symbol	Grade	Parameter	Condition	Min	Typical	Max	Uint
			Rising edge	-	2.54	-	
V_{LPD4}	2.65V	LPD threshold 4	Falling edge	-	2.64	-	
			Rising edge	-	2.74	-	
V_{LPD5}	2.85V	LPD threshold 5	Falling edge	-	2.84	-	
			Rising edge	-	2.94	-	
V_{LPD6}	3.05V	LPD threshold 6	Falling edge	-	3.05	-	
			Rising edge	-	3.15	-	
V_{LPD7}	3.25V	LPD threshold 7	Falling edge	-	3.25	-	
			Rising edge	-	3.35	-	

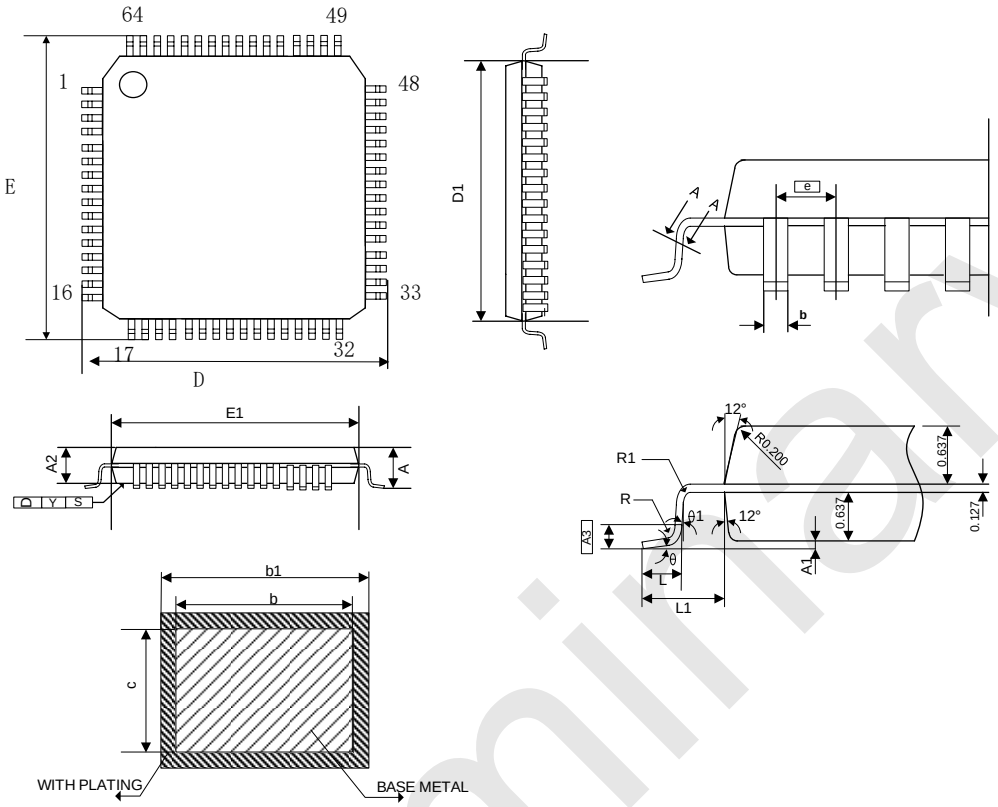
33 Package information

LQFP80 (12X12) Dimension (Unit: mm)



Symbol	mm(millimeter)		
	Min	Type	Max
A	1.40	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.18	-	0.26
b1	0.17	0.2	0.26
c	0.13	_	0.17
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
e	-	0.50 BSC	-
L	0.45	0.60	0.75
L1	-	1.00REF	-
θ	0°	3.5°	7°

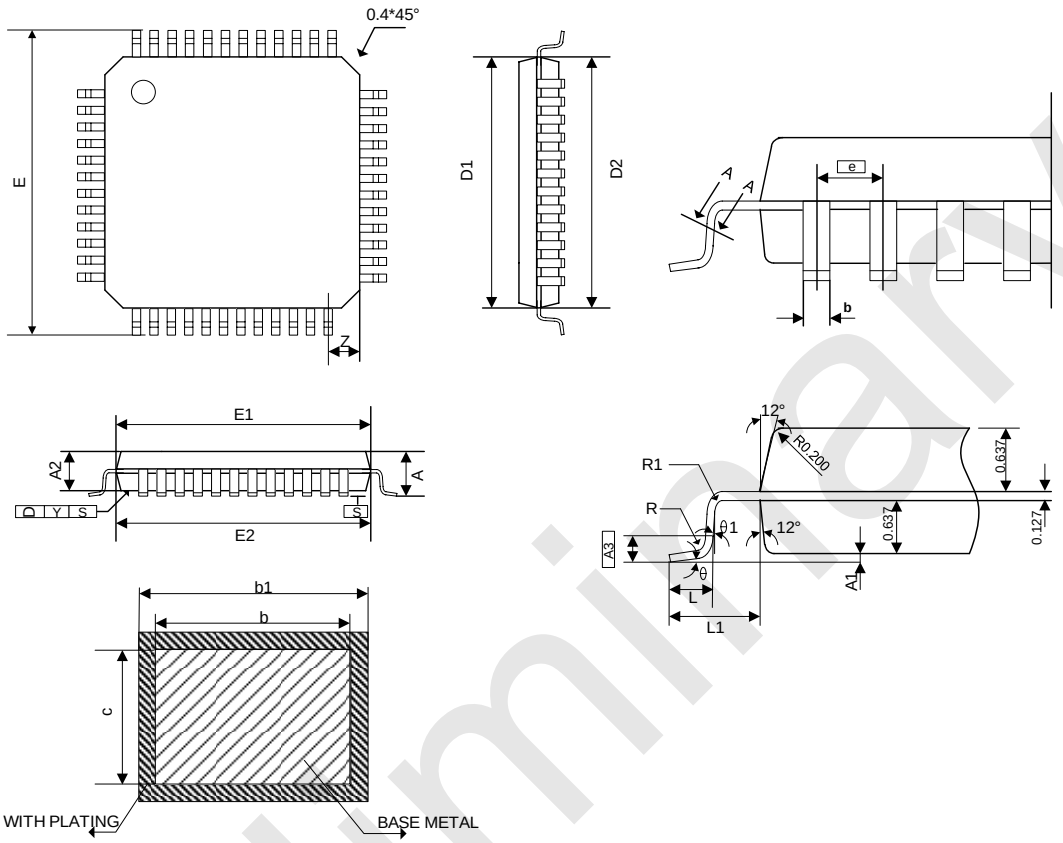
LQFP64 (10X10) Dimension (Unit: mm)



Symbol	mm(millimeter)		
	Min	Type	Max
A	1.40	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	-	0.23
b1	0.17	-	0.26
c	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	-	0.50 BSC	-
L	0.45	-	0.75
L1	-	1.00REF	-
R	0.08	-	-
R1	0.08	-	0.20

θ	0°	3.5°	7°

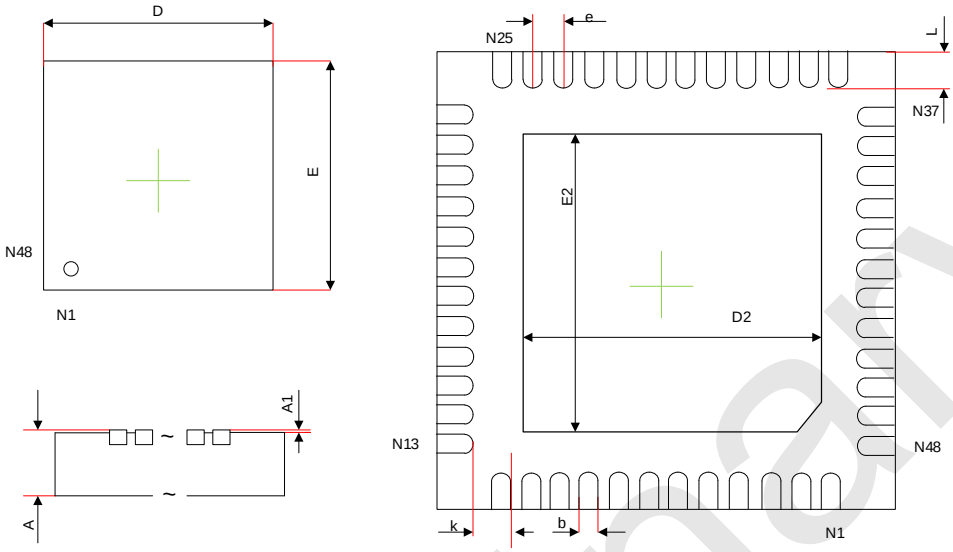
LQFP48 (7X7) Dimension (Unit: mm)



Symbol	mm(millimeter)		
	Min	Type	Max
A	1.45	1.55	1.65
A1	0.01	--	0.21
A2	1.30	1.40	1.50
A3	--	0.254	--
b	0.15	0.20	0.25
b1	0.16	0.22	0.28
c	0.12	--	0.17
D1	6.85	6.95	7.05
D2	6.90	7.00	7.10
E	8.8	9.00	9.20
E1	6.85	6.95	7.05
E2	6.9	7.00	7.10
e	--	0.5	--
L	0.43	--	0.75

Symbol	mm(millimeter)		
	Min	Type	Max
L1	0.90	1.0	1.10
R	0.1	--	0.25
R1	0.1	--	--
θ	0°	--	10°
θ1	0°	--	--
y	--	--	0.1
Z	--	0.75	--

LQFP48 (5X5) Dimension (Unit: mm)



Symbol	mm(millimeter)		
	Min	Type	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.12	--	0.23
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e	0.35 BSC.		
k	0.20	0.30	--
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40

34 Revision History

Version	Notes	Date
V0.1	Initial Release	2025.12.12

35 Important Notice

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